CHARACTERISATION AND APPLICATION OF MICROWAVE FIELD EFFECT TRANSISTORS.

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DECLARATION

The work described in this Thesis has not been submitted to any other University for a degree.

Some of the material presented has been published and copies of publications are included in the appropriate section.

Where use has been made of publications relevant to this work appropriate references have been given.

All other work and conclusions are those of the author unless otherwise stated.

SUMMARY

The work reported in this thesis is concerned with the determination of the microwave characteristics and possible applicatcns of Gallium Arsenide Field Effect Transistors at frequencies from 0.1 to 12 GHz. In order to characterise these active devices with reasonable accuracy and consistency the microwave network analyser facility at Warwick has been expanded and developed to give a 2-port, computer corrected, scattering parameter measurement capability. The resulting system has been tailored to the particular needs of GaAs FET characterisation and assessment, by the inclusion of subroutines which enable gain and stability parameters to be displayed in addition to the corrected s-parameters.

Various transistor package styles and corresponding test fixtures to enable the active devices to be interfaced with the network analyser have been investigated. Since the device test fixtures have used microstrip rather than co-axial transmission lines special calibration routines and standards have been developed to enable the computer correction system to be employed for the measurements.

Numerous devices have been characterised with the facility developed and the results used to establish the s-parameter characteristics of GaAs FETs at frequencies up to 12GHz. This information has been used to compare the predicted performance of different batches and types of device and in the design of circuits used to assess the actual performance of GaAs FETs in certain applications, such as small signal amplifiers and oscillators. Data on the effects of device processing and design changes on microwave performance have been fed back to the device manufacturer to aid optimisation of GaAs FET technology. Such measurements have shown the superior performance of aluminium versus nickel as a gate metallisation identified a weakness in electron beam fabricated devices and confirmed the advantage in using wider gate structures to lower impedances and simplify matching requirements.

S-parameter data for packaged FETs has been used to design amplifier and oscillator circuits which have been realised in order to assess the actual device performance in these applications. A comparison of predicted and measured performance at 3GHz has shown reasonable agreement. A novel tuning technique on microstrip was used to produce amplifiers at X-Band using chip devices. Using this technique with one micron gate length FETs a high gain (>40dB) amplifier at 11.2GHz was fabricated which confirmed the suitability of GaAs FETs as amplifier devices for such applications as high gain microwave amplifiers in repeater systems. At lower frequencies the GaAs FET has been shown to give excellent noise performance and is superior in this respect to bipolar transistors. The oscillator circuits incorporating GaAs FETs investigated exhibited two notable characteristics; good D.C. to R.F. conversion efficiency and poor noise and stability performance. The latter however, appears to result from the unoptimised nature of the circuits used.

In spite of some remaining unanswered questions, the overall conclusion from this investigation is that GaAs FETs, although relatively new devices (at the time of this study 1971-74) are useful solid state devices for numerous microwave applications. The importance of the GaAs FET in microwave systems has been underlined since the completion of this early study by the tremendous increase in activity in this field to the level seen today.

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C O N T E N T S

CHAPTER I.

Introduction.

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INTRODUCTION

1.1. General

The development of growth techniques for the compound (III-V) semiconductor materials in the 1960's opened the way to a new generation of active microwave devices. By the end of the decade one of these materials, Gallium Arsenide (GaAs), was being employed in Transferred Electron or Gunn Effect diodes, IMPATT diodes and for microwave frequency transistors. These transistors which are field effect devices consisting of a Schottky Barrier gate electrode controlling the current flow between ohmic source and drain contacts have been the subject of this investigation and thesis. The use of Gallium Arsenide is vital to the high frequency performance of the device. The high electron mobility and high carrier velocity, coupled with the use of semi-insulating Gallium Arsenide as the substrate material means that the GaAs FET will outperform its silicon counterpart by a factor of at least two.

1.2. Material Technology

Gallium arsenide technology is however more difficult than that for silicon and the development of a good, reliable GaAs material technology has proved an important factor in the fabrication of the FET. At the Allen Clark Research Centre of the Plessey Company where GaAs material and devices were pioneered processes for realising both have been developed. The semi-insulating GaAs substrate material is generally produced by doping pure GaAs with chromium. Epitaxial layers less than one micron thick, which are required to give devices with low operating voltages and good RF performance, are grown using Vapour Phase Epitaxy (VPE). This technique developed at Plessey by Knight et al (1) is an arsenic trichloride system and a schematic diagram of a typical growth equipment is shown in Fig. 1.1.

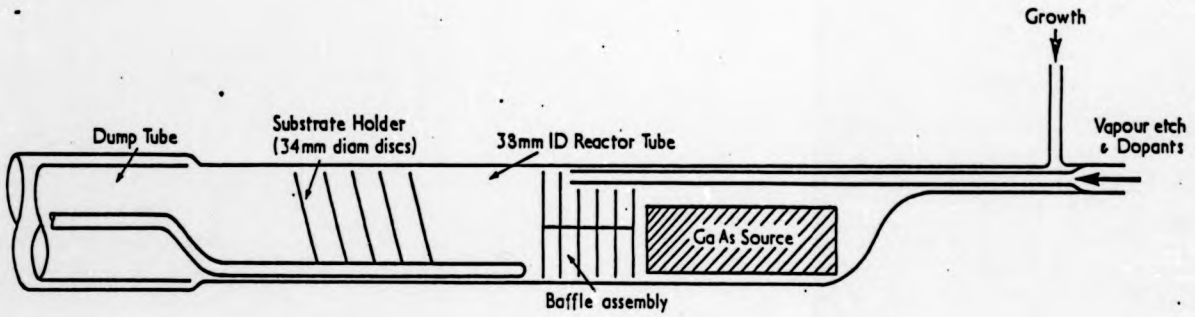


Fig: 1.1. Schematic of Vapour Epitaxy Reactor

This is an open tube gas flow system and has been developed for simplicity of use, the ease with which controlled amounts of doping impurity could be introduced to the growing epitaxial layers and its relatively rapid growth cycle.

Hydrogen is passed through a palladium-silver diffuser and on into a reservoir containing arsenic trichloride held at a controlled temperature below ambient. The arsenic trichloride is carried in the hydrogen stream into the first zone of the growth furnace where it reacts with the gallium arsenide source. This causes the formation of gallium chlorides which react with the excess arsenic in the system according to the equations below and gallium arsenide is formed.

$$6\ Ga\ Cl + As_4 \rightleftharpoons 4\ GaAs + 2\ Ga\ Cl_3$$

or

$$4\ Ga\ Cl + H_2 + As_4 \rightleftharpoons 4\ GaAs + 2\ HCl$$

Epitaxial growth on a gallium arsenide substrate placed in zone 2 can take place if the conditions within this zone are carefully controlled. If zone 2 is held at around 900°C, the arsenic trichloride will cause gallium arsenide to be removed from the surface of the substrate. If zone 2 is held at around 750°C epitaxial growth will proceed. By adjustment of the temperature of zone 2, therefore, it is possible to change from vapour etching to vapour growth. This ensures that epitaxial growth can always take place on a clean surface. This particular facility is most necessary in order to achieve the desired surface finish on the very thin layers required for the production of Gallium arsenide field effect transistors. In order to produce epitaxial material suitable for device fabrication it is necessary to introduce a doping impurity into the layer. The doping levels required for the FET are typically $5 \times 10^{16} - 10^{17}$ electrons/cm^3. This is achieved by passing purified hydrogen over heated crystals of sulphur to form hydrogen sulphide which is introduced into the growth furnace upstream of the gallium arsenide source.

Careful control of the temperature of the dopant and the flow rate of the hydrogen carrier gas determines the dopant impurity level in the growing layer. Tin doped epitaxial layers have also been produced by using a GaAs source doped with the required amount of tin. The advantage of tin is a lower diffusion coefficient which leads to a higher interface gradient at the n/semi-insulating interface. Fig. 1.2.

Processes have also been developed for the growth of semi-insulating epitaxial GaAs. This material has been used as a buffer layer between the substrate and the doped active layer in the FET structure. This prevents diffusion of impurities from the substrate into the active layer during the epitaxial growth process which can degrade the electrical parameters of the layer. To prevent contamination and unwanted doping during the growth processes strict controls of reagent purity and on the equipment environment are observed.

Following growth the GaAs wafer may be subjected to a number of characterisation techniques before being processed into FETs. The most used of these techniques is the plotting of Carrier Density Profiles for the wafer, information from which may be used to assess the suitability of the material for various device types.

1.3. Device Technology

Work on the GaAs FET has been in progress at the Allen Clark Research Centre since 1965. The original devices were produced using a diffused gate technology, but it soon became clear that this technology would be unacceptable for the production of high frequency devices due to the sideways spreading of the p-type zinc diffusant which limited the gate length to around two microns. However, the early results using this type of fabrication technology indicated that high frequency performance should be possible with suitably short gate lengths.

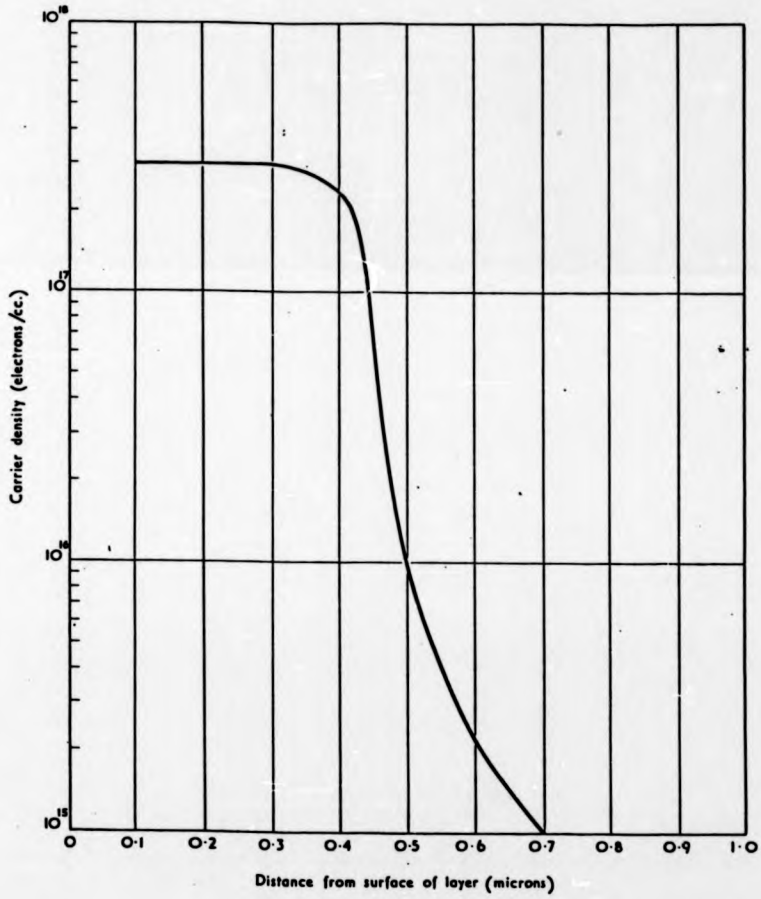


Fig. 1.2. Carrier density profile of tin doped epitaxial GaAs layer.

Since these early results, improvements in GaAs material parameters, the use of high resistivity buffer layers and of a Schottky barrier gate technology has led to the realisation of field effect devices having cut-off frequencies well into the microwave region.

Once the thin epitaxial layer has been produced, as described above, the fabrication of the FET is relatively simple compared to the complex processing technology of microwave bipolar transistors. The use of the Schottky barrier gate, a technology involving the use of a metal semiconductor diode as the control gate rather than the more conventional diffused gate diode, removed the need for any high temperature diffusion processes. The fabrication technology is thus reduced to two metal evaporation steps, one of In/Au/Ge alloy for the ohmic source and drain contacts and one of Al for the gate electrode and one isolation etch stage. The simplicity of the process is reflected in the reasonable yields obtained for even the shortest gate length devices.

In order to obtain high frequency operation from these devices it is necessary to produce a transistor with very short gate lengths. Classical field effect theory predicts that the frequency of operation is given by the expression $f_c \propto \mu/L^2$ where μ is the mobility of carriers in the channel region and L the length of the gate. This is however, only true for gate lengths in excess of about four microns. In short gate devices the electric fields in the channel region are so high that carriers reach their limiting velocities and the maximum frequency of operation is then determined by the transit time of the carriers in the channel region and this is given by the expression $f_c \propto V_m/L$ where V_m is the limiting velocity of carriers (2×10^{17}cm/sec for GaAs) and L is the effective channel length. Conventional photolithographic techniques are used to define devices with gate lengths down to two microns. For gate lengths shorter than two microns a more sophisticated technology is required. One micron gate lengths have been produced by both ultra violet projection printing and electron beam exposure techniques (4,5) but the limitations of the line resolution imposed

by the use of ultra violet radiation means that the shortest gate length structure will always be produced by the electron beam technology.

At Plessey an electron beam exposure technology has been developed that enables one micron gate length devices to be readily produced. In this technology the ohmic source and drain contacts are produced by conventional photolithographic techniques and only the gate is defined using the electron beam. The gate areas are defined by scanning a focussed beam of electrons across the slice on which an electron sensitive resist has first been applied. Fig. 1.3.

In both the conventional and electron beam technologies a 'float off' metallisation technique is used for producing the gate areas. In this technique resist is developed out of the gate areas and left in place on the remainder of the slice while the gate metal is evaporated all over the slice. The excess metal is then removed by placing the slice in a suitable solvent in which the dissolving resist will 'float off' taking the unwanted metal with it. Metal remains only in the gate areas.

Immediately prior to evaporation of the gate metal an etching process is used to define the channel thickness of the FET. The etching time required is determined by the thickness of the existing epitaxial layer (as determined from the carrier profile) and the gate pinch-off voltage required. This additional process step enables considerable latitude in initial layer thickness to be tolerated.

1.4. Assessment Techniques

After processing of the FET wafer has been completed the chips are subjected to visual inspection and electrical probe testing to sort good devices from failures. Failed devices typically exhibit faults such as incomplete gates, short circuits between electrodes or drain currents outside the acceptable range.

The resulting d.c. working FET chips are subsequently bonded into packages or mounted directly onto microstrip circuits for microwave assessment or

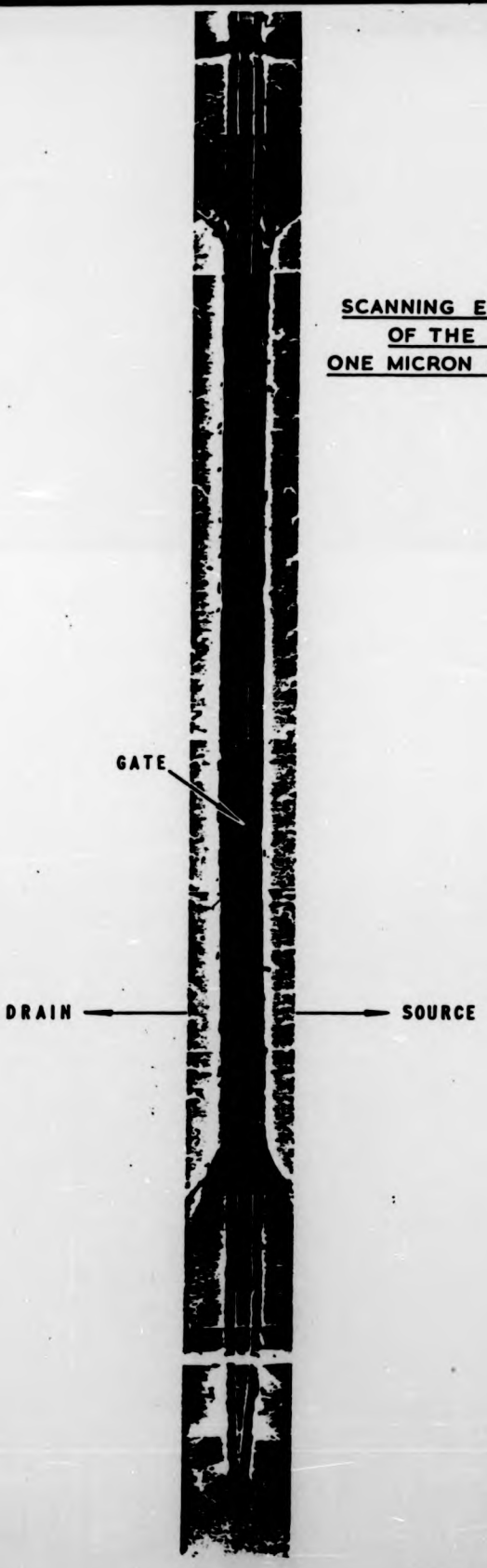


FIG 1.3

SCANNING ELECTRON MICROGRAPH OF THE GATE AREA OF A ONE MICRON GATE LENGTH GaAs FET

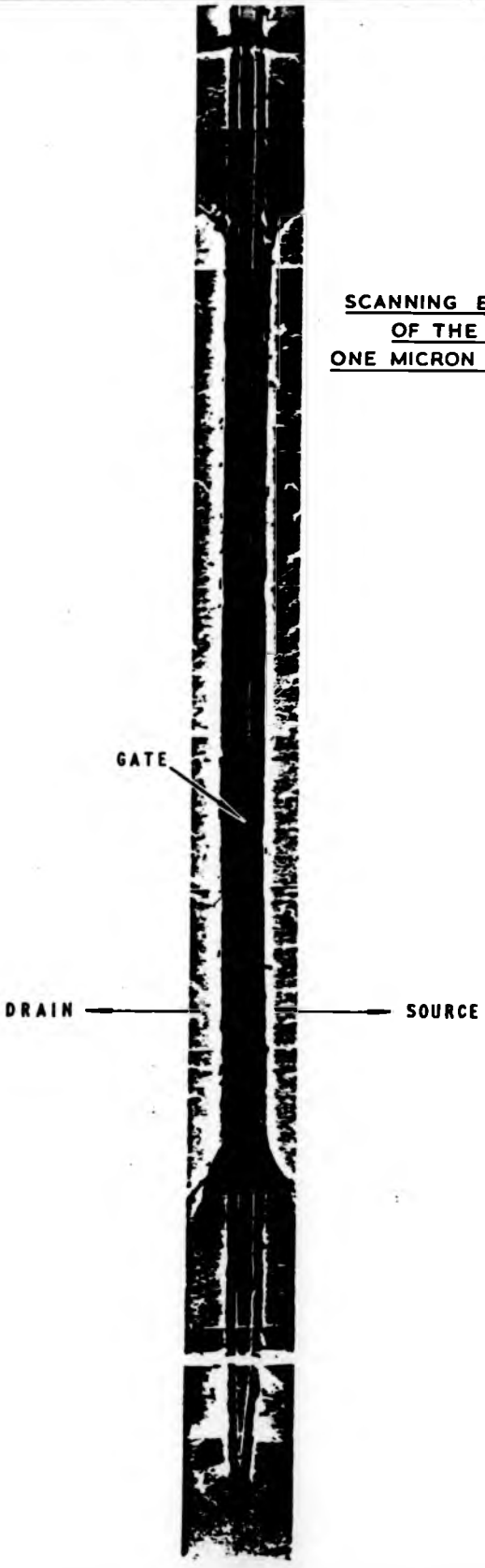


FIG.1.3

SCANNING ELECTRON MICROGRAPH OF THE GATE AREA OF A ONE MICRON GATE LENGTH GaAs FET

amplifier applications. When assessing the microwave performance the key parameters used are the gain and noise figure of the device at the frequency of interest. While both these parameters may be determined directly by placing the device in a test system with input and output variable tuning circuits such systems have to be used with care to prevent ambiguous results.(6)

Further data is required to define the overall characteristics of the FET and for this purpose the 'scattering' parameters are normally measured as a function of frequency. From these s-parameters the potential gain performance and other information relevant to amplifier applications may be readily calculated. Since the s-parameters can also be related to intrinsic characteristics of the FET they are especially useful in comparing effects of processing or other changes between batches of devices. During the course of this investigation a means of determining s-parameters of microwave FETs in various package configurations has been developed using computer correction techniques for improved measurement accuracy.(7). From the s-parameter and gain data obtained information has been fed back to the device manufacturer to aid design and process optimisation. The application of devices in various circuits has also been studied to confirm s-parameter predictions and to explore possible uses of the low noise GaAs field effect transistor.

CHAPTER II.

Transistor characterisation at microwave frequencies.

CHAPTER II

TRANSISTOR CHARACTERISATION AT MICROWAVE FREQUENCIES.

2.1. Scattering Parameters

At frequencies in excess of 1GHz microwave transistors are usually characterised by a set of 'black box' parameters known as scattering or S-parameters.

This set of parameters is analogous to the H, Y and Z parameters used at lower frequencies. The latter parameters are not normally used at microwave frequencies because they cannot be measured directly. This is because they are defined with the ports of the device open or short circuited. If such conditions are applied to microwave components the result is often instability and oscillation which precludes sensible measurement of the device. It is also difficult to measure total voltages and currents required for these parameters and to establish exact test conditions i.e. short and open circuits over a broad range of frequencies.

The significant difference with S-parameters is that they are measured with the device ports terminated by the characteristic impedance of the test system, usually 50 or 75 ohms for co-axial systems. Even with devices capable of operation to frequencies in excess of 10GHz instability problems seldom occur with such terminations hence permitting characterisation of the device. With S-parameters the magnitude and phase of travelling voltage waves rather than total voltages and total currents are measured. 'Scattering parameters' are so called because they relate those waves scattered or reflected from the network under test to those waves incident upon it.

The derivation of S-parameters and their relationship with H,Y and Z parameters is well covered in the literature H.P. Application Notes 95 and 154; K. Kurokawa 'Power Waves and the Scattering Matrix'; I.E.E.E. MTT-13 No.2 March 1965, and is not duplicated here.

In summary S-parameters offer the following advantages as a means of defining the performance of microwave transistors:

a) Using available equipment measurements can be made up to 18GHz.

b) Instability and parasitic oscillation of the device under test is minimised because of the broadband nature and characteristic impedance of the terminations.

c) Swept frequency measurements may be made instead of point-by- point methods.

d) They are easy to use for microwave circuit design and directly reflect the microwave performance of the device.

2.2. S-Parameter Measurement Technique

To fully describe a 2-port device the following parameters need to be determined with the device suitably terminated:

S_{11} - Input reflection coefficient = $\frac{E_{r1}}{E_{i1}}$

S_{21} - Forward Transmission = $\frac{E_{o2}}{E_{i1}}$

S_{12} - Reverse transmission = $\frac{E_{o1}}{E_{i2}}$

S_{22} - Output reflection coefficient = $\frac{E_{r2}}{E_{i2}}$

where E is the complex voltage, in (i), out(o) or reflected (r) at port 1 or port 2.

The most common means of measuring these complex ratios is by the use of a Network Analyser System such as the Hewlett Packard type 8410. This unit is a dual channel receiver which performs the function of a ratiometer between two signals and then displays these complex ratios on an output device. When appropriately interfaced with the device under test it is capable of displaying the above ratios and hence S- parameters directly.(8)

The interfacing is achieved by the use of test boxes or more conveniently for transistors by the use of an H.P. 8746B S-parameter test set. In addition to providing the necessary signal paths and switching to allow measurement of all four S-parameters, this unit also includes bias networks for the device under test and an input attenuator to reduce the incident power to the test device.(9)

In addition to the network analyser and test set a source of microwave energy at the frequency of interest is required. This is usually derived from a sweep oscillator allowing S-parameters to be displayed over a range of frequencies.

2.3. System Calibration

Having assembled a network analyser system and set it up appropriate to the frequency range and parameter of interest it first has to be calibrated before an unknown device may be measured. This calibration is achieved by the use of 'standard terminations'. For reflection measurements (S_{11} and S_{22}) the system is usually calibrated with a precision short circuit in place of the unknown.. With a swept RF input the system gain controls are adjusted to give unity reflection coefficient and the test box reference line adjusted for a constant phase of 180^{o}. The system is then giving the S_{11} of a perfect short circuit i.e. 1, 180^{o}.

The device of interest may then be connected and its reflection coefficient measured. For multiport devices the ports not connected to the test system must be terminated with matched loads of the same characteristic impedance as the test system. A similar calibration is needed for transmission parameters (S_{12}, S_{21}), but in this case the output and input ports of the system are connected to give a perfect 'through'. The system controls are then set to indicate the appropriate S-parameter indication namely $1,0^{o}$. This being completed an unknown device may be inserted and its transmission characteristics determined.

2.4. Calibration problems:

With a perfect network analyser system the above calibration procedures would be all that is required to obtain high accuracy, swept S-parameter measurements; however in practical test systems it is soon realised that this is not the case.

Calibration difficulties and measurement errors result from imperfections in the network analyser (type 8410A) indicator unit and the microwave components used to interface with the device under test. The latter is the major source of error when measuring the S-parameters of 2-port devices such as transistors, and is due to the following factors:

a) Mismatches within the S-parameter test set and transistor test fixture.

b) Finite directivity of directional couplers.

c) Dispersive effects in the system.

d) R.F. switch and attenuator repeatability.

Other errors result from imperfections in calibration standards, frequency uncertainties of the microwave source and the effects of noise on the measurement system. The end result is that measurements are inaccurate and have limited usefulness. In the case of GaAs FETs differences in parameters between devices and their absolute values can be completely masked by measurement errors rendering device characterisation and comparison impossible.

2.5. Computer corrected S-Parameter Measurements

The accuracy of network analyser measurements can be vastly improved by the use of correction routines which take account of system imperfections. This correction process involves characterising a number of known terminations over the frequency range of interest and using the measured characteristics of these terminations to determine error parameters of the measurement system. The effects of these errors are then subtracted from subsequent measured data to give corrected S-parameter information. (10)

This procedure is only practical over a swept frequency range if a computer is used to control the system, make the measurements required, store the data, calculate the corrected parameters and display the corrected results. At Warwick University a system has been developed using a XDS Sigma V computer on-line with a Hewlett Packard (8410A) Network Analyser to determine the S-parameters of GaAs FETs and amplifiers.

The heart of this system is the error model set up in the calibration process. The approach followed has been based on that due to Hand (11) but modified to allow the use of optional calibration standards and full 2-port correction without the necessity of physically reversing the device under test. Considering a simple two port system first for measuring FETs or amplifiers the test unit will consist of an 'unknown' port to which the input is connected and behind which two directional couplers sample the incident (reference) and the reflected (test) signal. In addition a 'Return' port is available to which the device output is connected. Switching allows the transmitted (test) signal to be measured by a common receiver.

The error model set up in the calibration process includes the effects of the microwave test unit and also some of the errors due to the network analyser.

2.6. The Calibration Process

The calibration process involves making sufficient measurements with standards of known characteristics to determine the error parameters. The various model coefficients are identified on the signal flowgraph of the system model Fig. 2.1. The S-parameters of the device connected between the unknown and return ports are represented by S_{11}, S_{21}, S_{12}, S_{22} in the usual way. Using flowgraph analysis the following general expressions for the measured values of reflection (M_R) and transmission (M_T) coefficients are obtained:

$$M_R = e_{00} + \frac{S_{11}\, e_{01}\,(1 - S_{22}\, e_{22}) + S_{21}\, S_{12}\, e_{22}\, e_{01}}{1 - S_{11}\, e_{11} - S_{22}\, e_{22} - S_{21}S_{12}e_{11}e_{22} + S_{11}e_{11}S_{22}e_{22}} \qquad 1.$$

$$M_T = e_{30} + \frac{S_{21}\, e_{32}}{1 - S_{11}e_{11} - S_{22}e_{22} - S_{21}S_{12}e_{11}e_{22} + S_{11}e_{11}S_{22}e_{22}} \qquad 2.$$

Calibration measurements with standard terminations to determine the the error parameters are made as follows:

a) Reflection with a sliding load. The reflection as connected is measured and then repeated three times after being re-positioned by the operator. The computer then calculates the centre of the circle passing through these points so that effectively $S_{11} = 0$. S_{21} and S_{12} are also zero since the unknown and return ports are not connected. From equation (1),

$$M_1 = e_{00}$$

b) Transmission without a through connection, both ports terminated. This sets $S_{11} = S_{21} = S_{12} = S_{22} = 0$ and so from equation (2),

$$M_2 = e_{30}$$

c) Reflection with a direct short circuit,

Sets, $S_{11} = -1$; $S_{21} = S_{12} = S_{22} = 0$ so,

$$M_3 = e_{00} - \frac{e_{01}}{1 + e_{11}}$$

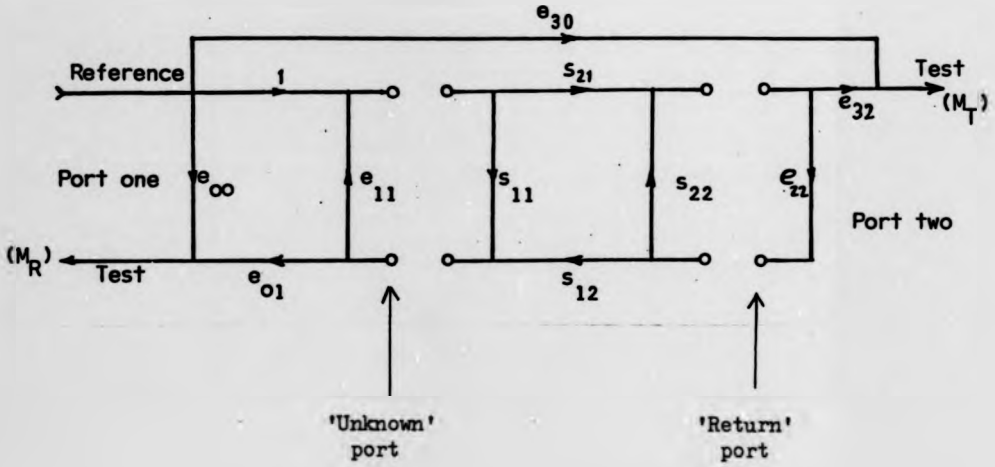


Fig. 2.1. Signal flowgraph of system model.

d) Reflection with an offset short circuit of length l (approximately $\lambda/4$ at midband).

$S_{11} = -e^{-j2\beta l} = T_s$ for convenience

and $S_{21} = S_{12} = S_{22} = 0$ so,

$$M_4 = e_{00} + \frac{T_s\ e_{01}}{1 - T_s\ e_{11}}$$

e) Reflection with a through connection.

Sets $S_{11} = S_{22} = 0$, and $S_{21} = S_{12} = 1$ so,

$$M_5 = e_{00} + \frac{e_{22}\ e_{01}}{1 - e_{11}e_{22}}$$

f) Transmission with a through connection.

Sets as (e) $S_{11} = S_{22} = 0$ and $S_{21} = S_{12} = 1$, so

$$M_6 = e_{30} + \frac{e_{32}}{1 - e_{11}e_{22}}$$

These six equations can be rearranged to give the error parameters from the measured results. When solved by the computer this gives the required error model parameters:

$$e_{00} = M_1$$

$$e_{11} = \frac{T_S\ (M_1 - M_3) + (M_1 - M_4)}{T_S(M_3 - M_4)}$$

$$e_{01} = \frac{(1 + T_S)(M_1 - M_3)(M_1 - M_4)}{T_S(M_3 - M_4)}$$

$$e_{30} = M_2$$

$$e_{22} = \frac{M_5 - M_1}{e_{01} + (M_5 - M_1)\ e_{11}}$$

$$e_{32} = (M_6 - M_2)\ (1 - e_{11}\ e_{22})$$

After the calibration these six values are calculated and stored for use in correcting subsequent measurements.

2.7. Device Measurement Process

With the unknown device connected reflection and transmission measurements are made and then the device is reversed and the two measurements repeated. From equations (1) and (2):

$$M_{R1} = e_{00} + \frac{S_{11}e_{01}(1 - S_{22}e_{22}) + S_{21}S_{12}e_{22}e_{01}}{D_1}$$

$$M_{T1} = e_{30} + \frac{S_{21}e_{32}}{D_1}$$

where $D_1 = 1 - S_{11}e_{11} - S_{22}e_{22} - S_{21}S_{12}e_{11}e_{22} + S_{11}e_{11}S_{22}e_{22}$

and $$M_{R2} = e_{00} + \frac{S_{22}e_{01}(1 - S_{11}e_{22}) + S_{12}S_{21}e_{22}e_{01}}{D_2}$$

$$M_{T2} = e_{30} + \frac{S_{12}e_{32}}{D_2}$$

where $D_2 = 1 - S_{22}e_{11} - S_{11}e_{22} - S_{12}S_{21}e_{11}e_{22} + S_{22}e_{11}S_{11}e_{22}$

2.8. Device S-parameter determination

After the measurement the computer solves the above equations for S_{11}, S_{21}, S_{12} and S_{22} using the stored error parameter values. The S-parameters are derived using an iterative process which has negligible error since an explicit solution to the expressions is prohibitively complex. The corrected S-parameters are stored after calculation so that they may be recalled in different display modes or dumped onto magnetic tape for subsequent analysis.

2.9. Two Port Correction Procedure

The necessity to reverse the device under test with the above procedure, section 2.7, slows down the measurement process and with active devices can cause problems with bias supplies. To overcome these disadvantages a 2-port routine was developed by the authorbased on the previous procedure but in which the functions of the 'Unknown' and 'Return' ports are interchanged by switches within the H-P8746B S-parameter test set. Thus while the device need not be reversed some additional error parameters do have to be determined. These are obtained by similar calibration runs to those described above. The signal flowgraph representing the complete system is shown in Fig. 2.2. (a) and (b).

The s-parameters of any device connected between the two ports are represented by S_{11}, S_{21}, S_{12}, S_{22}. The properties of the test unit, plus some of the errors due to transmissions and mounting arrangements, are represented by the e-parameters, which are not assumed to be independent of the reference port. Flowgraph analysis results in the following general expressions for the measured values of reflection and transmission coefficients:-

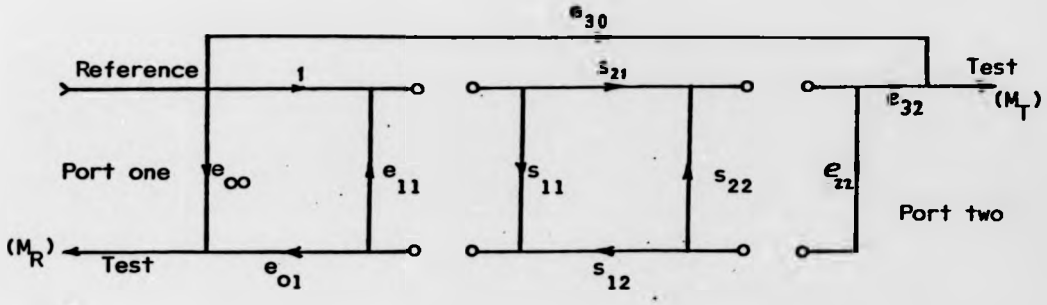
$$M_R = e_{oo} + \frac{S_{11}e_{01}(1 - S_{22}e_{22}) + S_{21}S_{12}e_{22}e_{01}}{1 - S_{11}e_{11} - S_{22}e_{22} - S_{21}S_{12}e_{11}e_{22} + S_{11}e_{11}S_{22}e_{22}}$$

$$M_T = e_{30} + \frac{S_{21}e_{32}}{1 - S_{11}e_{11} - S_{22}e_{22} - S_{21}S_{12}e_{11}e_{22} + S_{11}e_{11}S_{22}e_{22}}$$

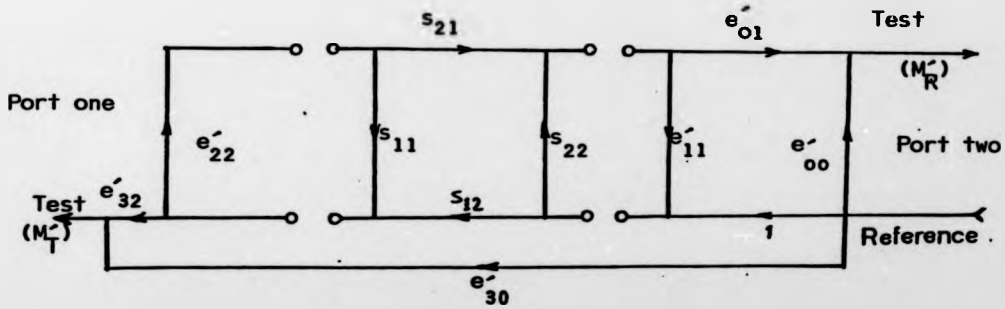
$$M_R' = e_{oo}' + \frac{S_{22}e_{01}'(1 - S_{11}e_{22}') + S_{12}S_{21}e_{22}'e_{01}'}{1 - S_{22}e_{11}' - S_{11}e_{22}' - S_{12}S_{21}e_{11}'e_{22}' + S_{22}e_{11}'S_{11}e_{22}'}$$

$$M_T' = e_{30}' + \frac{S_{12}e_{32}'}{1 - S_{22}e_{11}' - S_{11}e_{22}' - S_{12}S_{21}e_{11}'e_{22}' + S_{22}e_{11}'S_{11}e_{22}'}$$

The calibration process involves making sufficient measurements with standard terminations and under definable conditions to determine all of the e-parameters.



(a) Port one as reference.



(b) Port two as reference

FIG. 2.2. Signal flowgraphs of two-port system.

Calibration

The calibration measurements involve the following:-

(a) Reflection with a sliding load.

The computer measures the reflection three times, instructing the user to slide the load between measurements. It then constructs a circle passing through the three values and finds the centre of the circle. Thus

$$S_{11} = S_{21} = S_{12} = S_{22} = 0 .$$

Hence

$$M_1 = e_{oo}, \qquad M_1' = e_{oo}'$$

(first port) (second port)

(b) Transmission without a "through connection", both measurements ports terminated.

$$S_{21} = S_{12} = 0$$

Hence

$$M_2 = e_{30}, \qquad M_2' = e_{30}'$$

(c) Reflection with a short circuit or off-set short circuit.

$S_{11} = -e^{-j2\beta\ell}$, where ℓ is the length of the off-set short circuit.

Again, $S_{21} = S_{12} = 0$

and it follows that

$$M_3 = e_{oo} + \frac{Ae_{01}}{1-Ae_{11}} ,$$

where

$A = -e^{-j2\beta\ell}$ for an off-set short circuit

$A = -1$ for a short circuit ($\ell = 0$)

Similarly, for $S_{22} = -e^{-j2\beta\ell'}$, $S_{21} = S_{12} = 0$

leads to

$$M_3' = e_{oo}' + \frac{A'e_{01}'}{1-A'e_{11}'} .$$

(d) Reflection with an off-set short or open circuit.

Here

$$S_{21} = S_{12} = 0$$

$$S_{11} = -e^{-j2\beta\ell} \quad \text{for an off-set short circuit}$$

$$= e^{-j2\theta} \quad \text{for an open circuit, where } \theta = \tan^{-1}(\omega C Z_o) .$$

Hence

$$M_4 = e_{oo} + \frac{Be_{01}}{1-Be_{11}} ,$$

where

$$B = -e^{-j2\beta\ell} \quad \text{for an off-set short circuit}$$

$$= e^{-j2\theta} \quad \text{for an open circuit}$$

Similarly, for $S_{22} = -e^{-j2\beta\ell'}$ or $e^{-j2\theta'}$, $S_{21} = S_{12} = 0$ and one obtains

$$M_4' = e_{oo}' + \frac{B'e_{01}'}{1-B'e_{11}'} ,$$

(e) Reflection with a 'through' connection.

Here

$$S_{11} = S_{22} = 0, \qquad S_{21} = S_{12} = e^{-j\beta\ell} ,$$

where ℓ is the 'through' length

Letting $L = e^{-j\beta\ell}$ $\quad (L = 1 \text{ if } \ell = 0)$

leads to

$$M_5 = e_{oo} + \frac{L^2 e_{22} e_{01}}{1-L^2 e_{11} e_{22}}$$

and

$$M_5' = e_{oo}' + \frac{L^2 e_{22}' e_{01}'}{1-L^2 e_{11}' e_{22}'}$$

(f) Transmission with a 'through' connection

Now $S_{11} = S_{22} = 0$, $S_{21} = S_{12} = e^{-j\beta\ell}$

where again ℓ is the 'through' length

Hence

$$M_6 = e_{30} + \frac{Le_{32}}{1-L^2 e_{11} e_{22}}$$

and

$$M_6' = e_{30}' + \frac{Le_{32}'}{1-L^2 e_{11}' e_{22}'} .$$

The equations for $M_1 \rightarrow M_6$ and $M_1' \rightarrow M_6'$ can be solved to give the desired e-parameters:

Letting
$$X_1 = M_3 - M_1$$
$$X_2 = M_4 - M_1$$
$$X_3 = M_4 - M_3$$
$$X_4 = M_5 - M_1$$
$$X_5 = M_6 - M_2 \quad ,$$

it follows that:

$$e_{oo} = M_1$$

$$e_{11} = \frac{AX_2 - BX_1}{ABX_3}$$

$$e_{01} = \frac{X_1X_2(B-A)}{ABX_3}$$

$$e_{30} = M_2$$

$$e_{22} = \frac{X_4}{L^2(e_{01} + X_4e_{11})}$$

$$e_{32} = \frac{X_5(1 - L^2e_{11}e_{22})}{L} \quad .$$

Similar equations can be obtained for e_{oo}', e_{11}', e_{01}', e_{30}', e_{22}', e_{32}'. Different e-parameters are obtained for each frequency point and used by the computer for correcting all subsequent measurements at that frequency. Values for A, B and L are computed from information provided by the user.

Device Measurments

When a device of unknown parameters is connected to the system, reflection and transmission measurements are made at each port. Re-writing the expressions for M_R and M_T :

$$M_R = e_{oo} + \frac{S_{11}e_{01} + e_{01}e_{22}(S_{21}S_{12} - S_{11}S_{22})}{D} \qquad (3)$$

$$M_T = e_{30} + \frac{S_{21}e_{32}}{D} \quad , \qquad (4)$$

where $D = 1 - S_{11}e_{11} - S_{22}e_{22} - e_{11}e_{22}(S_{21}S_{12} - S_{11}S_{22})$

Similarly,

$$M_R' = e_{oo}' + \frac{S_{22}e_{01}' + e_{01}'e_{22}'(S_{21}S_{12}-S_{11}S_{22})}{D'} \quad (5)$$

$$M_T' = e_{30}' + \frac{S_{12}e_{32}'}{D'} \quad , \quad (6)$$

where $D' = 1 - S_{22}e_{11}' - S_{11}e_{22}' - e_{11}'e_{22}'(S_{21}S_{12}-S_{11}S_{22})$

Letting $Q = S_{21}S_{12} - S_{11}S_{22}$, it follows from Eqns (3)...(6) that

$$S_{11} = \frac{(M_R-e_{oo})D}{e_{01}} - e_{22}\,Q \quad (7)$$

$$S_{21} = \frac{(M_T - e_{30})D}{e_{32}} \quad (8)$$

$$S_{22} = \frac{(M_R' - e_{oo}')D'}{e_{01}'} - e_{22}'\,Q \quad (9)$$

$$S_{12} = \frac{(M_T' - e_{30}')D'}{e_{32}'} \quad (10)$$

An explicit solution to eqns 7 to 10 , although theoretically feasible, is unnecessary and an iterative method of solution is used, which has been shown to have negligible error. The procedure is as follows:

Initially set

$$\hat{S}_{11} = M_R \quad \hat{S}_{21} = M_T \quad \hat{S}_{22} = M_R' \quad \hat{S}_{12} = M_T'$$

Then:

(1) Calculate Q, D, D' from $\hat{S}_{11}$, $\hat{S}_{21}$, $\hat{S}_{22}$, $\hat{S}_{12}$ and the e-parameters.

(2) Calculate new values for $\hat{S}_{11}$, $\hat{S}_{21}$, $\hat{S}_{22}$, $\hat{S}_{12}$ as follows:

$$\hat{S}_{11} = \frac{(M_R - e_{oo})D}{e_{01}} - e_{22}Q \qquad \hat{S}_{21} = \frac{(M_T - e_{30})D}{e_{32}}$$

$$\hat{S}_{22} = \frac{(M_R' - e_{oo}')D'}{e_{01}'} - e_{22}'Q \qquad \hat{S}_{12} = \frac{(M_T' - e_{30}')D'}{e_{32}'}$$

(3) Return to (1)

This cycle is repeated until a convergence is obtained.

The final values for $\hat{S}_{11}$, $\hat{S}_{21}$, $\hat{S}_{22}$ and $\hat{S}_{12}$ are the corrected S-parameters for the unknown device.

Relationships Between Measurement Parameters

The relationship between the reading sequence of the 2-port correction programme and the measurement parameters is given below.

Programme K setting	Type of measurement	Device to be measured	Equation Parameters
1	S_{11}	sliding load	M_1
2	S_{11}		
3	S_{11}		
4	not used		
5	S_{22}	sliding load	M_1'
6	S_{22}		
7	S_{22}		
8	not used		
9	S_{21}	matched termination	M_2
10	S_{12}	matched termination	M_2'
11	S_{11}	Short-or offset short circuit	M_3
12	S_{22}	offset-or open circuit	M_4
13	S_{22}	offset-or open circuit	M_3'
14	S_{11}	Short-or offset short circuit	M_4
15	S_{11}	'Through' Connection	M_5
16	S_{21}		M_6
17	S_{22}		M_5'
18	S_{12}		M_6'
19	S_{11}	Device under Test	M_R
20	S_{21}		M_T
21	S_{22}		M_R'
22	S_{12}		M_T'

CHAPTER III.

Implementation of an on-line correction system.

CHAPTER III

IMPLEMENTATION OF AN ON-LINE CORRECTION SYSTEM

3.1. Basic Requirements

In applying computer correction to microwave measurements the major problem to be resolved is the interfacing between the computer and the microwave equipment. At Warwick this was further complicated by the physical separation of the computer and microwave systems. The Sigma V computer was used because it was available on site, had ample computing power and was well supported with input/output and other peripheral devices. Various interface units to interconnect the Sigma V computer with the Hewlett Packard 8410A network analyser have been developed. A computer programme written in Fortran IV has been produced which handles the necessary calculations, control and display functions involved with 2-port correction measurements. (Appendix 1)

3.2. System Interfacing

Interfacing to the computer can be divided into three basic functions. These are:

1. Programme input commands and output display.
2. Network analyser control commands.
3. Data acquisition from network analyser.

The functions are implemented via cables connecting the microwave and computer rooms. A single multiconductor screened cable satisfies function (1) by enabling a Tektronix Visual Display Unit (VDU) to operate remotely from the computer. This is used by the operator to control the execution of the programme and by the computer to output instructions and display data.

The functions involving the network analyser, 2. and 3. use ten twisted pair cables which also connect the microwave and computer rooms. The limited number of lines available has meant the adoption of techniques which maximise their use.

For instance by serialising 8-bit parallel data the information may be transmitted using a pair of lines rather than the eight otherwise required. The interface units required and their relation to the network analyser system are shown in the system block diagram Figure 3.1.

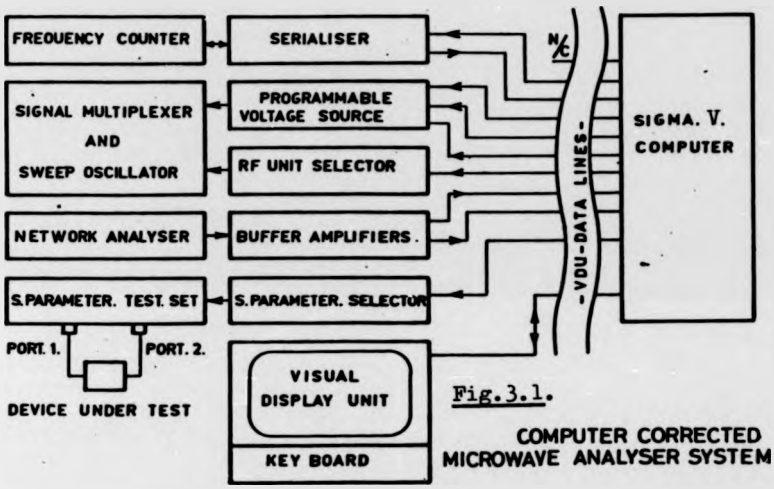


Fig.3.1.

COMPUTER CORRECTED MICROWAVE ANALYSER SYSTEM

3.3. Network Analyser/Computer Interface Units

a) Serialiser

Converts the parallel output from the Hewlett Packard 5340A frequency counter into serial form and gives control commands to the counter. This is achieved using 2 lines to the computer and the circuit shown, Figure 3.2. This consists of TTL and operational amplifier integrated circuits to decode control and clock pulses received at connector CPR.1 and to output status and data information at connector CPR.2. In use CPR.1 is connected to an analogue output of the Sigma V computer. A negative voltage results in the generation of counter control commands RFD and DAC via Op-amp 'A'. (12) Positive voltage pulses are routed through Op-amp 'B' to produce clocking pulses for the serialiser.

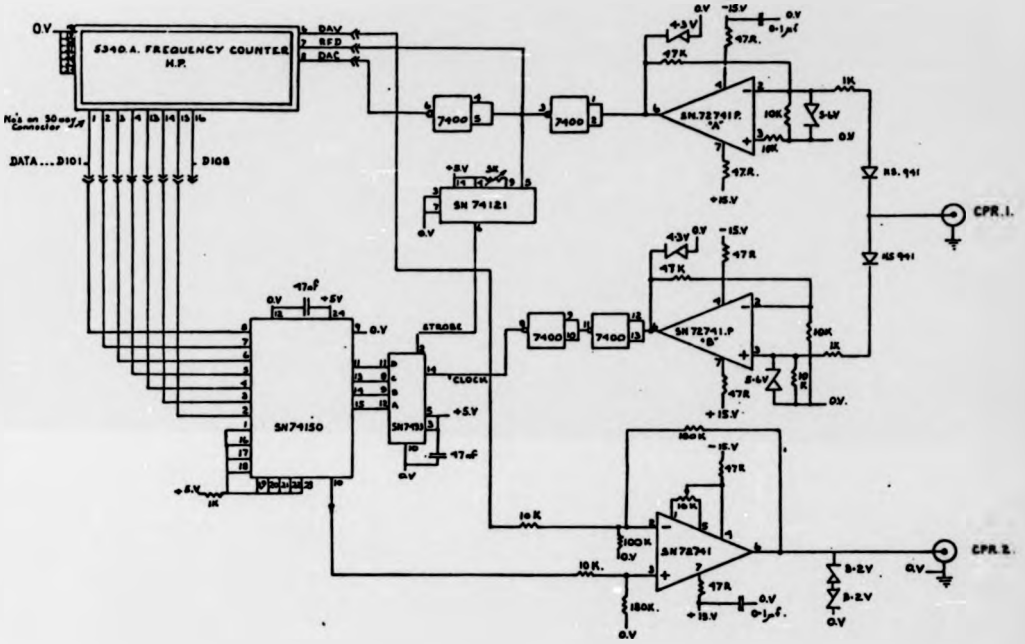


FIG. 3.2. Parallel to serial data convertor circuit diagram.

The operational amplifiers 'A' and 'B' are connected as high gain comparators with input overload protection and series diodes for noise immunity. A further Op-amp is used to buffer outputs to connector CPR2 which is connected to an analogue input of the computer. The status (DAV) of the counter is transmitted as a positive output while data pulses are negative going. Clamping diodes across the buffer output ensure the $\pm$ 10V input limit of the analogue input is not exceeded. By using analogue rather than digital ports of the computer each line carries two sets of information distinguished by polarity. Routines within the computer programme determine the amplitude (nominally $\pm$ 5V) plus timing of the counter interrogation signals and read the returning data.

b) Programmable Voltage Source

This unit generates the precision tuning voltage for the microwave source to select the required output frequency. The tuning voltage may be varied from +3 to +73 volts, the normal sweep oscillator ramp range in one millivolt steps. This interface was custom built by a commercial company for use with the automated network analyser system. Three lines from analogue outputs of the computer connect to the unit. Pulses received on one line are counted and increment the output voltage when a 'transfer' pulse is received on a second line. The third line is used for a 'reset' pulse which sets the output back to the starting voltage. This starting voltage is normally +3 volts but is switch selectable to 0V if desired. (13)

c) RF Unit Selector

Selects the appropriate sweep oscillator unit for the frequency of interest as instructed by an analogue signal from the computer. The sweep oscillator units, mounted in the Hewlett Packard 8707A Multiplexer unit are selected by a BCD coded input. A discrete component analogue to digital converter was designed and built to generate the required BCD code from a single analogue input signal. Figure 3.3 .

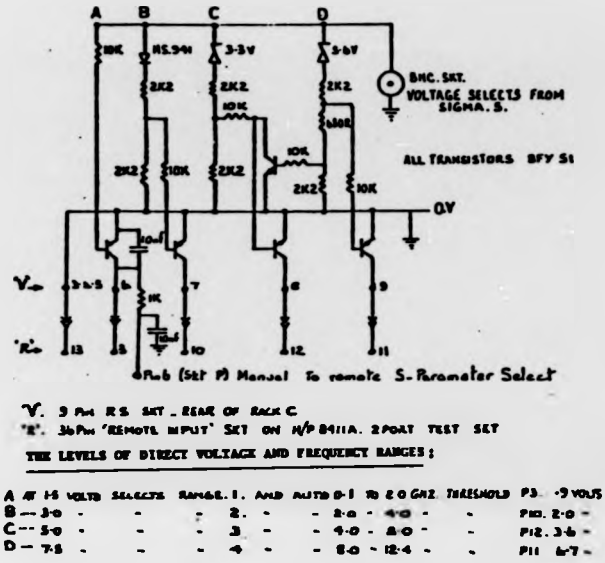


Fig. 3.3. RF Unit selector interface circuit.

Thus one line and output from the computer handles the frequency band selection.

d) Buffer Amplifiers

Two 741 operational amplifiers connected as d.c. amplifiers with voltage gains of ten times serve to amplify and buffer the analogue outputs from the network analyser. Amplifying these outputs before connecting them to the co-axial lines improves the noise immunity of the system and the resolution which can be obtained from the computer analogue inputs.

e) S-Parameter Selector

This interface is similar to the RF Unit selector (c) in that a single analogue output voltage from the computer is converted to the necessary 3-bit binary code to select the S-parameter to be measured.

3.4. System Operation

In order to achieve repeatable and accurate measurements it is essential that each time the system is used a number of requirements are satisfied. For instance:

1. The microwave, interface and computer parts must be correctly connected and set up.
2. The system must be stable and not subject to drift.
3. The computer programme and peripheral units have to be loaded and functioning correctly.

In view of the complex nature of the computer corrected system, where possible steps have been taken to reduce the possibility of errors occurring during setting up which could lead to erronious data and wasted measurement runs. To this end the interface units have been designed, where possible, to allow them to be left permanently connected to the microwave equipment. When not connected to the computer the system automatically reverts to the manual operating mode. The microwave network analyser units are also permanently connected so that the only major setting up required is that associated with the system gain and the S-parameter test set. The latter may require adjustment of the Reference Channel length depending on the nature of the device under test. Figures 3.4 to 3.6.

With the final system the only action required to link the microwave system to the computer is the patching of the interconnecting lines to the computer input/output ports and the connection of the multiway VDU cable, both operations being carried out in the computer room. To minimise thermal drift in the microwave equipment it is switched on and allowed to stabilise preferably for at least an hour before attempting measurements.

Provided there are no problems with the computer the correction programme is loaded, usually from magnetic tape and a second data tape to receive data from the programme when measurements are made is installed in the tape unit.

FIG. 3.4.

Network analyser test station at Warwick University.

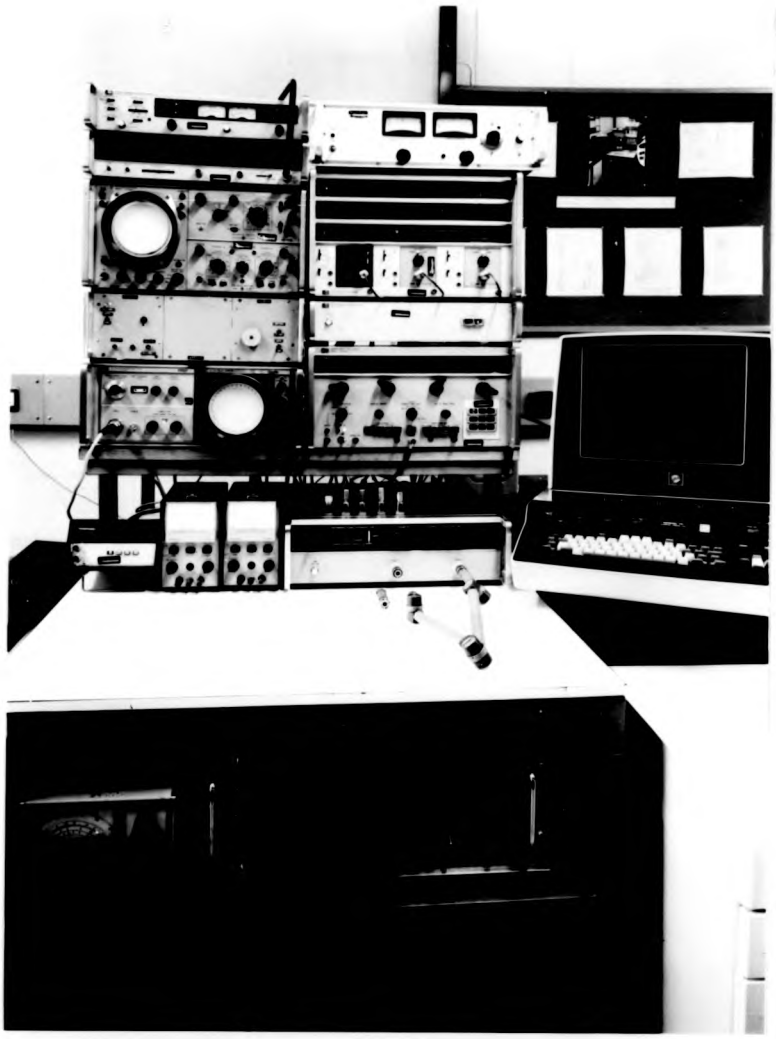


FIG. 3.4.

Network analyser test station at Warwick University.

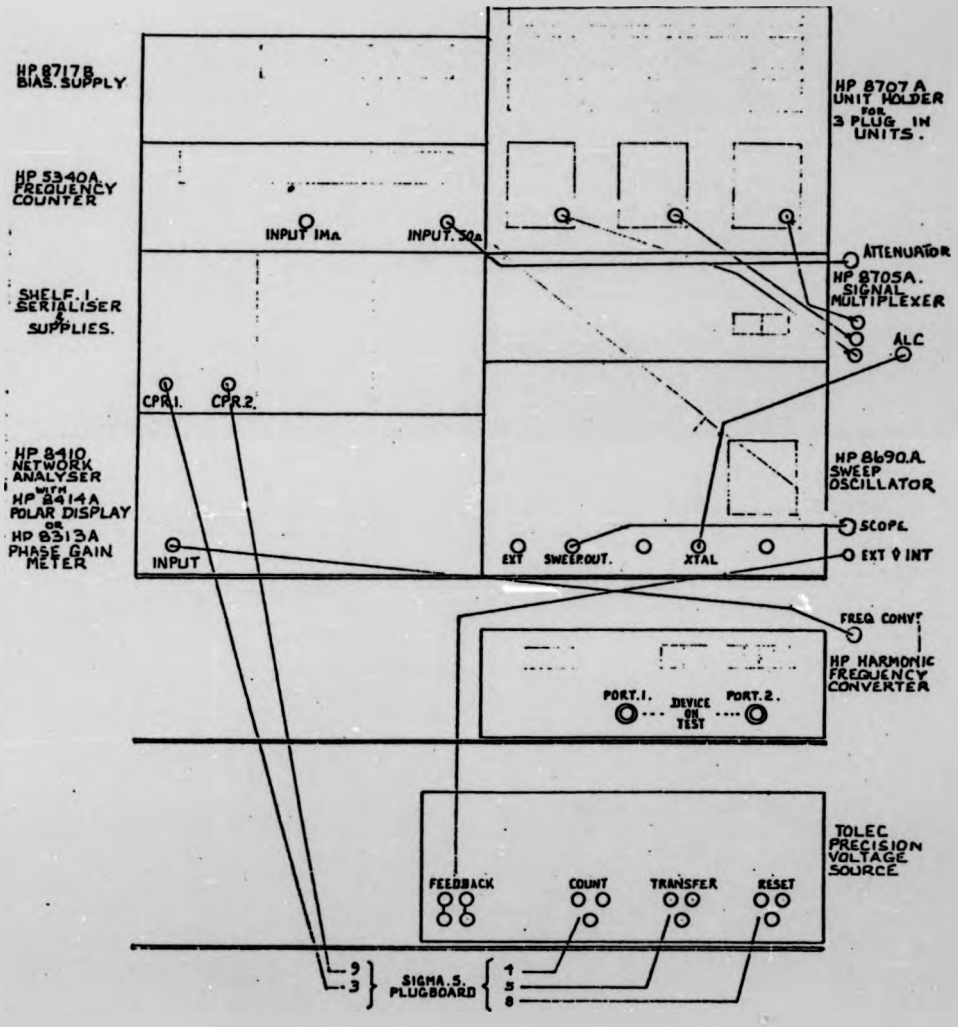


FIG. 3.5.

Block diagram of front view of network analyser showing interconnections.

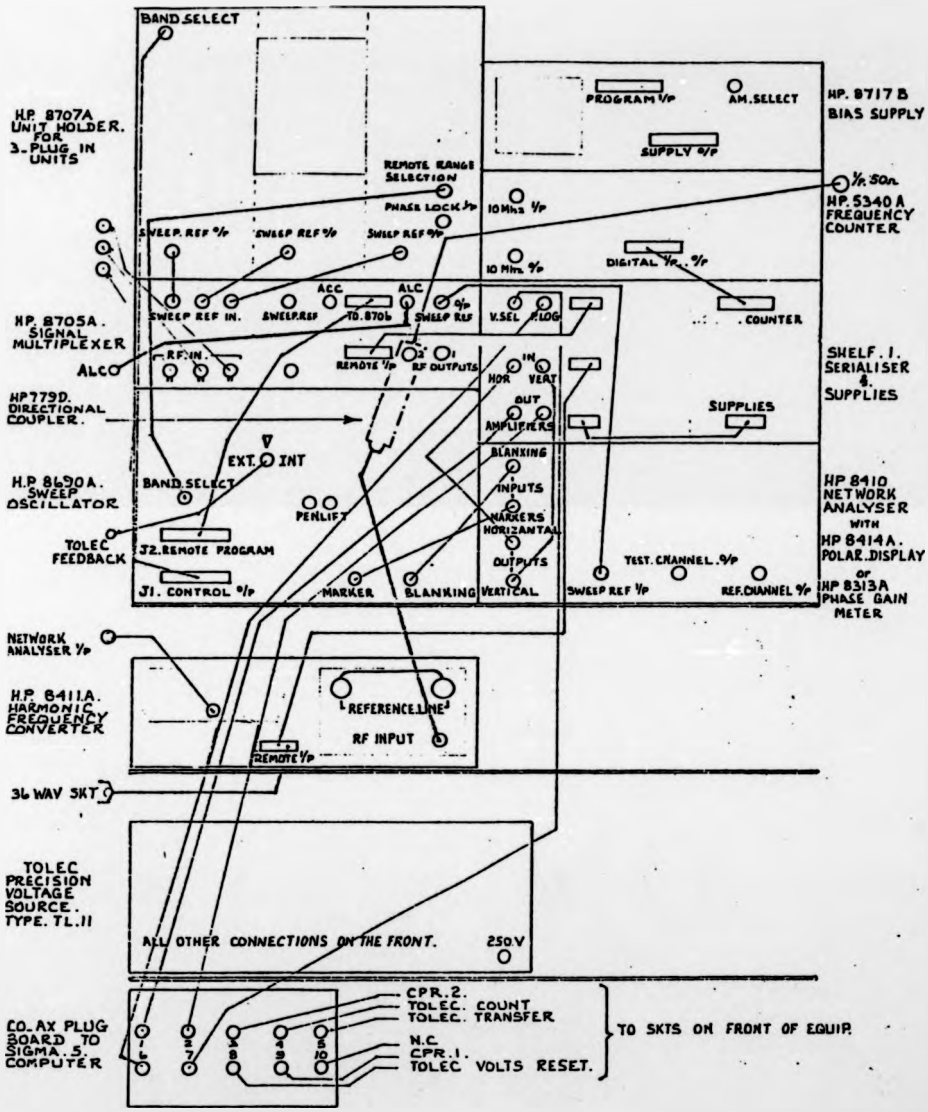


FIG. 3.6.

Block diagram of rear view of network analyser showing interconnections.

On running the programme a message is displayed on the VDU to confirm that the required data tape is correctly in position. In operation the computer performs operations as instructed by the operator via the VDU and its input keyboard. A set of instructions for two port correction, with typical responses is shown Figure 3.7.

The questions appear on the screen one at a time and after each one the computer waits until there is entered on the keyboard either a number followed by a 'carriage return' or a 'Y' which is automatically completed to a 'YES' on the screen, or an 'N' which is likewise completed to a 'NO'. The answer is stored and the next question appears. The various procedures in the calibration routine are identified by the 'K' values 1-15, which facilitates the repeating of any particular stage. This can be effected by typing 'N' in response to a question, whereupon the VDU displays 'TASK?' The typing of 'SK' at this stage permits a repeat run corresponding to any particular selection of K, which is then entered. The full set of options available under 'TASK?' is shown in the list of Figure 3.8 which is displayed on the VDU in response to typing the letters 'LI'. The subsequent entering of any of the listed letter pairs will permit the related function to be accomplished.

In addition to responding to prompts from the computer the operator is required to connect the required calibration pieces and finally the device to be tested. If any of the measurement runs are suspect they may be repeated by the use of the 'TASK?' instruction.

```
2-PORT FULL CORRECTION PROGRAM
ARE AMPLIFIERS IN USE ? TYPE Y OR N YES
WAVEGUIDE OR COAX - TYPE W OR C '' COAX
LENGTH OF OFFSET SHORT  CM. = 1.0
IS JOYSTIK IN USE ? TYPE Y OR N NO
NO. OF POINTS PER READING   10
TIMING INTERVAL (N   0.01 SEC).  N = 30
INPUTS TAKEN FROM POLAR DISPLAY OR PHASE GAIN UNIT
TYPE LOG. LIN. OR POL  POL
CENTRE BEAM WHILE TYPING ANY CHARACTER k
MAXIMUM FREQUENCY (GHZ) = 2.0
MINIMUM FREQUENCY (GHZ) = 1.0
NO. OF POINTS = 5
MINIMUM FREQUENCY SET UP
CORRECTION TO FREQ. IN MHZ = N.N
CORRECTION TO FREQ. IN MHZ = 0

K=1   CONNECT MATCHED LOAD''YES
K=2   SLIDE LOAD''YES
K=3   SLIDE LOAD''YES
K=4   SLIDE LOAD''YES
K=5    CONNECT MATCHED LOAD''YES
K=6    SLIDE LOAD''YES
K=7    SLIDE LOAD''YES
K=8    SLIDE LOAD''YES
K=9    FWD TRANSM  2 MATCHED LOADS''YES
K=10   REV TRANSM  2 MATCHED LOADS''YES
K=11   S/C ON PART 1''YES
K=12   OFFSET SHORT ON PORT  2''YES
K=13   SHORT CIRCUIT ON PORT 2''YES
K=14   OFFSET SHORT ON PORT 1''YES
K=15   CONNECT THRO LINE''YES
NEW DEVICE? ''YES
IDENTIFY DEVICE & TERMINATE WITH CR
TEST RUN ONLY

K=19   CONNECT DEVICE''
```

Fig. 3.7. Instructions for 2-Port Correction.

```
TASK    (TYPE L1 FOR LIST OF OPTIONS) ''
TASK OPTIONS - TWO LETTER KEYS REQUIRED
L1   LIST OPTIONS            ZE  RESTART PROGRAM
BG   RESTART CALIBRATION     RE  REPEAT LAST READING
SK   RESET K (SEE BELOW)     ND  GO TO NEW DEVICE
CA   CALCULATE               PR  PRINT
DI   ENTER DISPLAY           DU  DUMP READINGS
UD   UNDUMP READINGS         ST  RELEASE PROGRAM
CO   INSERT COMMENT          CE  CENTRE BEAM
AM   RESET AMPLIFIERS        IN  RESET INPUT TYPE
WA   WAVEGUIDE OR COAX       CL  DEFINE CALIB PIECES
JO   JOYSTICK SWITCH         FR  RESET FREQ RANGE
MF   CORRECT MIN FREQ        NO  RESET NO. POINTS
TI   RESET TIMING INT        TP  UPDATE TAPE FORMAT
DC   DISC FILE CLEAR


SETTINGS FOR K IN SK OPTION
K=1   CONNECT MATCHED LOAD ON PORT 1
K=2   SLIDE LOAD
K=3   SLIDE LOAD
K=4   SLIDE LOAD
K=5   CONNECT MATCHED LOAD ON PORT 2
K=6   SLIDE LOAD
K=7   SLIDE LOAD
K=8   SLIDE LOAD
K=9   FWD TRANSM  2 MATCHED LOADS
K=10  REV TRANSM  2 MATCHED LOADS
K=11  SHORT CIRCUIT ON PORT 1
K=12  OFFSET SHORT 1 ON PORT 2
K=13  SHORT CIRCUIT ON PORT 2
K=14  OFFSET SHORT 1 ON PORT 1
K=15  CONNECT THROUGH LINE

K=19  CONNECT DEVICE
```

Fig. 3.8. 'TASK' Operations.

The results of the measurement run may be displayed in various ways on the VDU, printed on a line printer or stored on magnetic tape for subsequent processing and analysis. When measuring a number of devices, as is the case when assessing parameter spreads, it is desirable to complete the measurements as quickly as possible to avoid errors due to equipment drift. In such a case the data would be dumped to magnetic tape immediately and subsequently recalled for assessment.

The effectiveness of the correction routine may be seen from the results for a known device such as a through connection between the test ports. The corrected and uncorrected reflection and transmission amplitudes, (S_{11}, U_{11} and S_{12},U_{12} respectively) for a through line are shown Fig. 3.9. From the uncorrected (connected) points corrected values of unity transmission and zero reflection are obtained. Similarly Fig. 3.10 shows the uncorrected and corrected phase angles.

While such results with known devices are impressive it is the application of the same technique to unknown elements enabling them to be fully assessed which is the important feature of computer corrected network analyser systems.

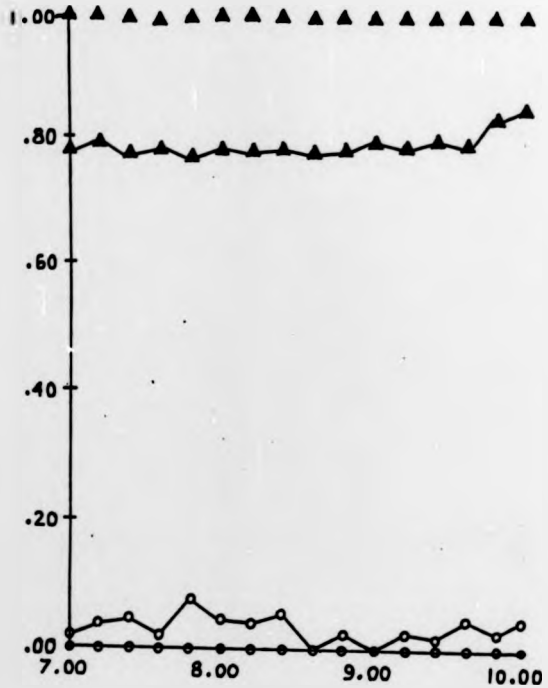


Fig. 3.9. Corrected (S_{11},S_{12}) and measured (U_{11},U_{12}) parameters of a 'through' line.

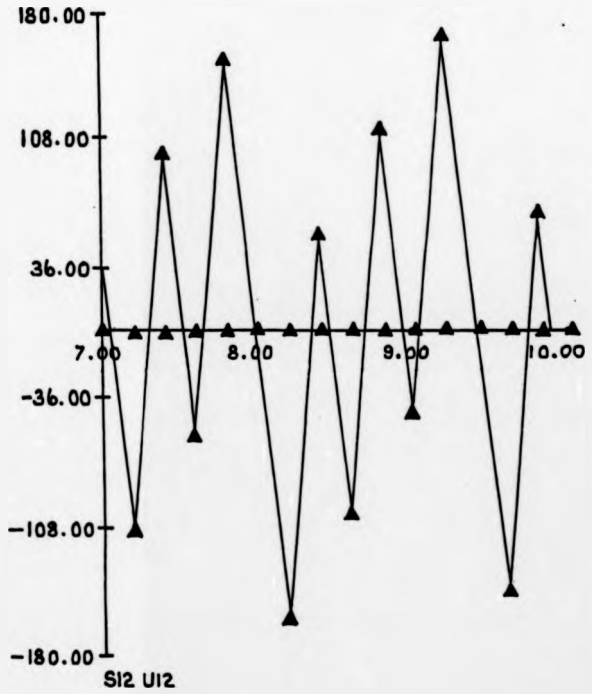


Fig. 3.10. Corrected (S_{12}) and measured (U_{12}) reverse transmission phase angles of a 'through' line.

CHAPTER IV.

Transistor test fixtures.

CHAPTER IV

TRANSISTOR TEST FIXTURES

In order to assess and compare packaged devices suitable test fixtures are required. These fixtures need to satisfy a number of requirements:

a) The device source must be efficiently grounded.

b) Devices must contact consistently.

c) Reference planes must be definable.

d) Good microwave performance.

e) Ease of device changing.

Often compromises have to be made because of differing package styles so that not all the requirements can be met.

4.1. Test fixture parameters

a) Source Grounding

In the usual package configuration the source is the common terminal of the FET. For measurement and many application purposes the source contact of the FET must be connected directly to ground by as low an impedance path as possible. If this is not done the device parameters or the performance of a circuit will be degraded. With a packaged device problems arise from the common source inductance which is ever present. This is made up principally of three parts.

1. The source bond wire inductance.
2. The inductance associated with the package common terminal.
3. The inductance of the package grounding arrangement.

Factors 1 and 2 are determined and fixed in a particular package however, 3 can be minimised by suitable mounting configurations.

b) Contact consistency

When various devices have to be measured for comparitive purposes or the same device has to be remeasured it is obvious that a sound contact must be made between the package leads and the fixture each time. Any loss due to poor contacts will degrade the measured S-parameters and if variable device to device will make performance comparisons difficult if not impossible. It must also be appreciated that from device to device contact between the package leads and the fixture must be at the same point otherwise phase errors occur. At 10GHz with an alumina test fixture if a device is incorrectly positioned by 0.1mm then an error in phase on a polar plot of over 5^{o} will result. Precision positioning and contacting to the device under test is thus required. The situation can be eased slightly by the use of low dielectric constant substrates or air line which reduces the effective electrical lengths of positioning errors.

c) Reference plane definition

Unless reference plane positions can be accurately defined in the measurement jig the system calibration will be in error and so will any subsequently determined device parameters. It is vital that the system calibration is adequate if sensible measurements are to be made.

The reference plane positions are usually defined using 'standard' terminations such as precision short circuits and through connections. It is however, often difficult to realise such ideal calibration terminations in a fixture designed to receive a transistor package and alternative terminations or calibration procedures may have to be found. With all microwave transistor test assemblies, calibration of the system and the establishment of reference planes is the most

difficult yet vital requirement since all other measurements hinge on it.

d) Microwave performance

While error correction routines can remove effects of microwave shortcomings in test fixtures where possible these should be avoided. To this end transitions between co-axial and microstrip lines and to transistor packages need to be optimised to keep VSWR's low. Also where connections between the test fixture and measurement equipment are to be made precision connectors such as APC-7 should be used.

With a through line installed the transistor test fixture should have the lowest possible insertion loss and VSWRs. Similarly with no device in the fixture the isolation between the input ports should be high, preferably $>$ 20dB if significant errors are to be avoided in the reverse transmission S_{12} of devices.

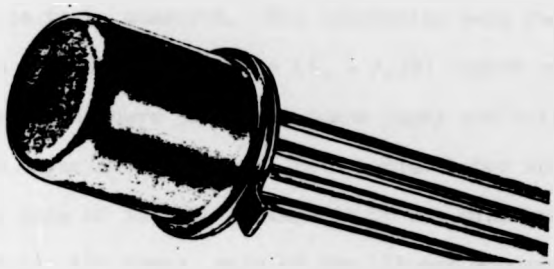
e) Ease of device changing

In order to compare performance of devices from different production batches it is necessary to characterise several devices from each batch. It should therefore be possible to remove and insert devices into the test fixture relatively easily to minimise measurement time. This reduces the possibility of errors resulting from drift of the measurement system between calibration and test runs.

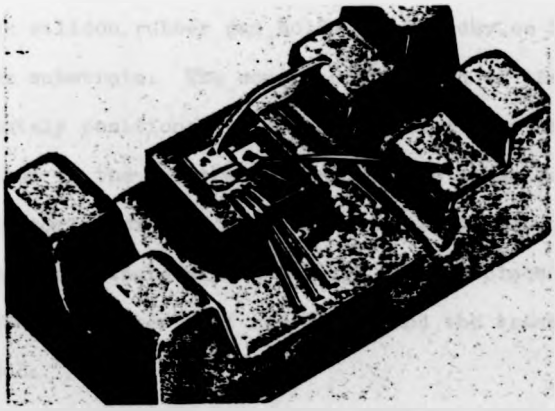
In practice even with fixtures which enable devices to be changed quickly the actual time taken by the computer controlled network analyser to fully characterise a transistor over an octave bandwidth will be less than that required to change transistors!

4.2. Package styles and test fixtures used

During this investigation GaAs FETs have been evaluated in the following packages.



1. TO-72, conventional 4-lead transistor can.
   This package which is usable up to about 1.5GHz has been employed for low frequency device assessment and applications. The device S-parameters were measured using a commercial test fixture made by General Radio who also supply appropriate through and shorted lines for calibration purposes.



2. Leadless Inverted Device (LID) package.
   An early microwave transistor package the LID is usable to ~ 10GHz and has been used extensively for the characterisation and comparison of one micron gate length FETs.

For assessment of LID packaged devices a purpose built fixture was developed from an unmachined Hewlett Packard type 11608A transistor jig. Fig. 4.1.

Two substrate and ground plane configurations were produced for use in this to enable the scattering parameters of LID devices to be measured. The substrates were fabricated from 0.023 inch thick Polyguide ($\epsilon_r = 2.32$) copper clad dielectric material and have 50ohm impedance input and output lines which taper at the ends to form contacts for the gate and drain pads of the LID package(14) On one substrate (type A Fig.4.2) the source pads of the LID are grounded by a large pad on the surface of the substrate which wraps round the edge of the dielectric to contact the ground plane on the back while on the other (type B, Fig.4.2) part of the brass ground plane passes through a hole in the substrate to provide a more direct ground for the device source contact (Requirement a).

The transistor jig lid was modified so that when closed a single silicon rubber pad holds the LID device in position on the substrate. The source contact end of the package is accurately positioned by a locating slot in a metal plate attached to the substrate surface. The S-parameters of the transistor mount were measured over the frequency range 8-12GHz for each substrate with a through line in place of a LID device. The VSWR of either port was < 1.35 and the transmission loss < 0.4dB.

Initial measurements using both substrate configurations revealed that the direct grounding configuration (Substrate type B) reduces the magnitude of the reverse transmission, S_{12}, of the device under test and this leads to an increase in the maximum stable gain (MSG).

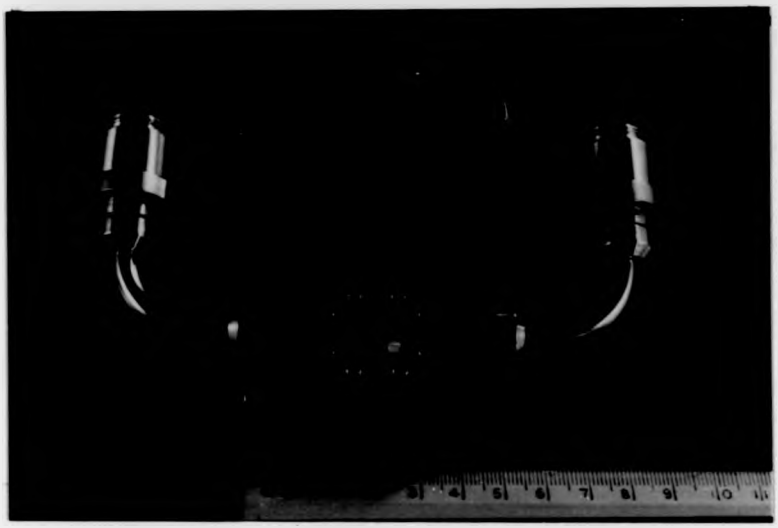


FIG. 4.1.

Hewlett Packard Transistor fixture,

modified for LID packages.

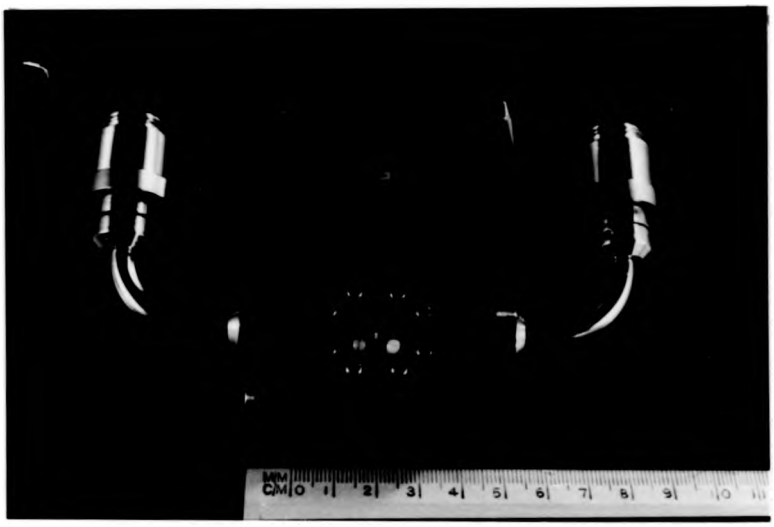


FIG. 4.1.

Hewlett Packard Transistor fixture,

modified for LID packages.

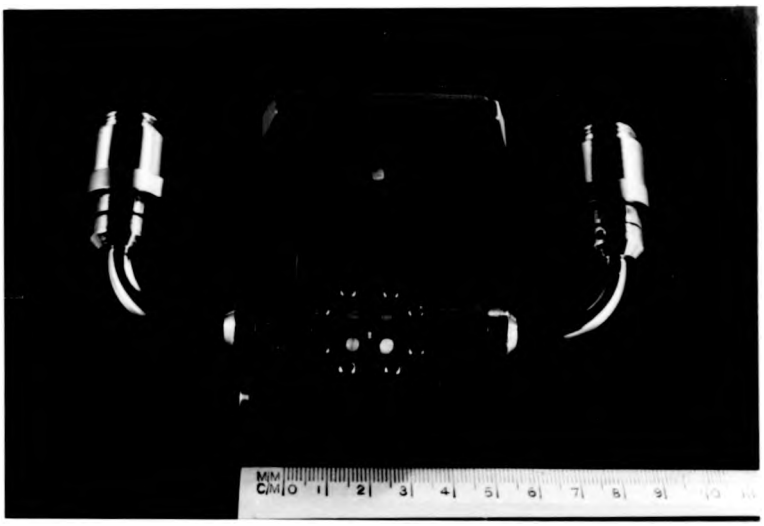


FIG. 4.1.

Hewlett Packard Transistor fixture,

modified for LID packages.

LID MOUNTED TRANSISTOR JIG IN POLYGUIDE

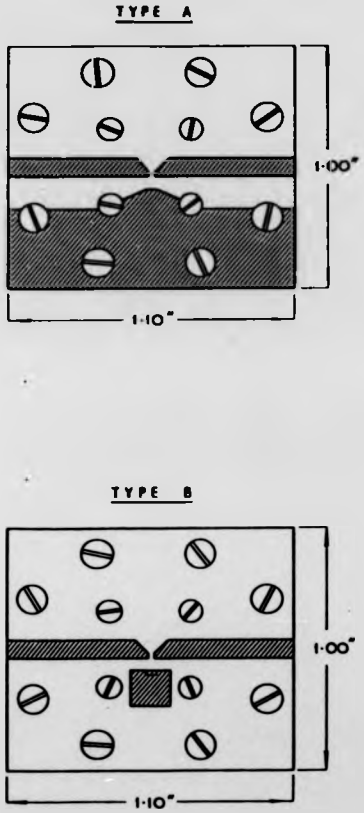
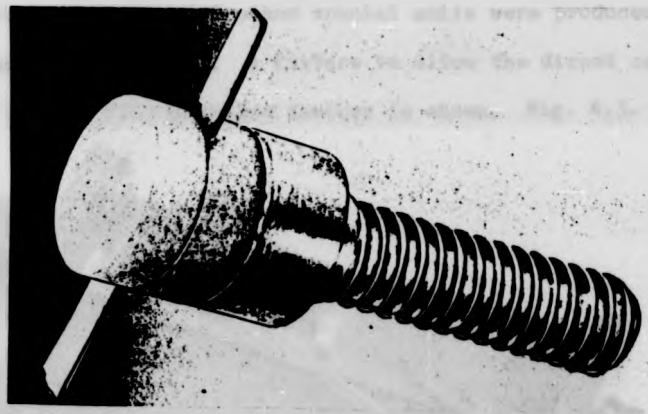


FIG. 4.2. LID package test substrates and package configuration.

At 12GHz the improvement in the MSG is typically 3dB. Apart from the degradation of S_{12} due to the extra source inductance the other S-parameters of devices measured at X-Band with both substrate configurations were very similar.

After the above preliminary measurements the direct grounding configuration was adopted permanently in this LID test fixture for subsequent use.



3. Microstrip Studded Package, P103.

Because of inadequacies of the LID package especially at higher frequencies various alternatives were studied. A commercial package the P103 met this need and was adopted for packaging GaAs FETs.

Being a new package with a threaded stud no commercial test fixtures existed for this and it was not compatible with existing designs. A simple, but effective measurement fixture design was produced for this device using 0.25 inch aluminium backed Polyguide substrates to which SMA coaxial to microstrip connectors were bolted. The P103 package dropped into a flat bottomed hole in the substrate and was held in place by a nut on its threaded stud.

For calibration purposes a second substrate, shorter than the first by the package size, with a through microstrip line was used. The P103 package and its test fixture is superior to the LID due to better source grounding and greater isolation between input and output ports. All the test fixtures were used with the computer controlled network analyser for device S-parameter characterisation. In addition a number of other special units were produced for package experiments. A fixture to allow the direct comparison of LID and P103 packaged devices is shown. Fig. 4.3.

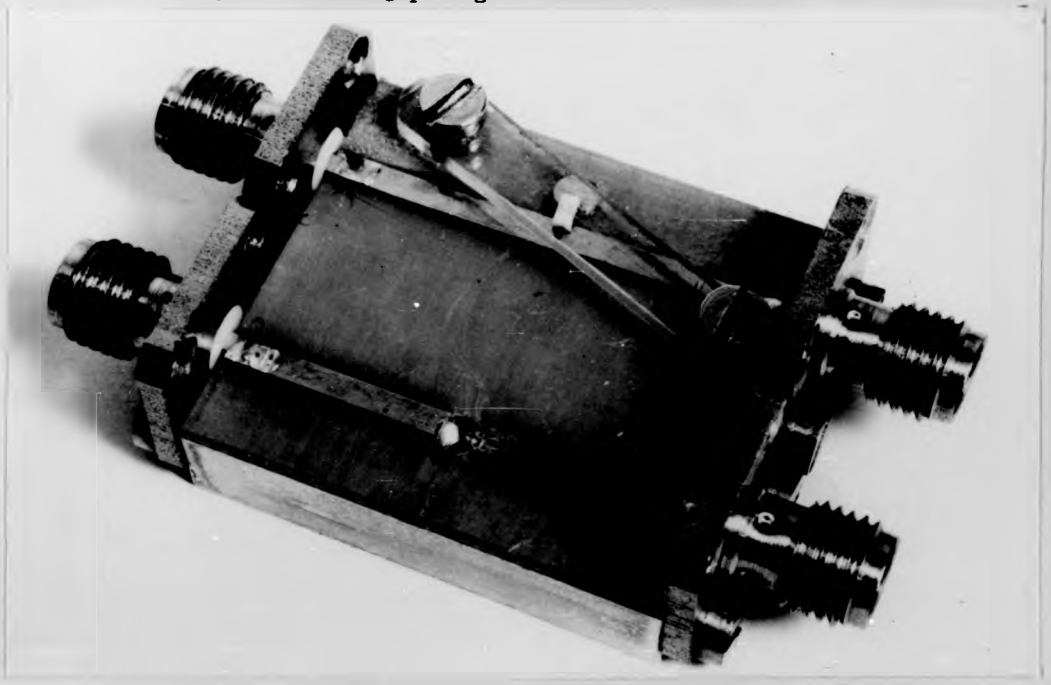


FIG. 4.3. Polyguide test fixture for the comparison of LID and P103 packages.

For calibration purposes a second substrate, shorter than the first by the package size, with a through microstrip line was used. The P103 package and its test fixture is superior to the LID due to better source grounding and greater isolation between input and output ports. All the test fixtures were used with the computer controlled network analyser for device S-parameter characterisation. In addition a number of other special units were produced for package experiments. A fixture to allow the direct comparison of LID and P103 packaged devices is shown. Fig. 4.3.

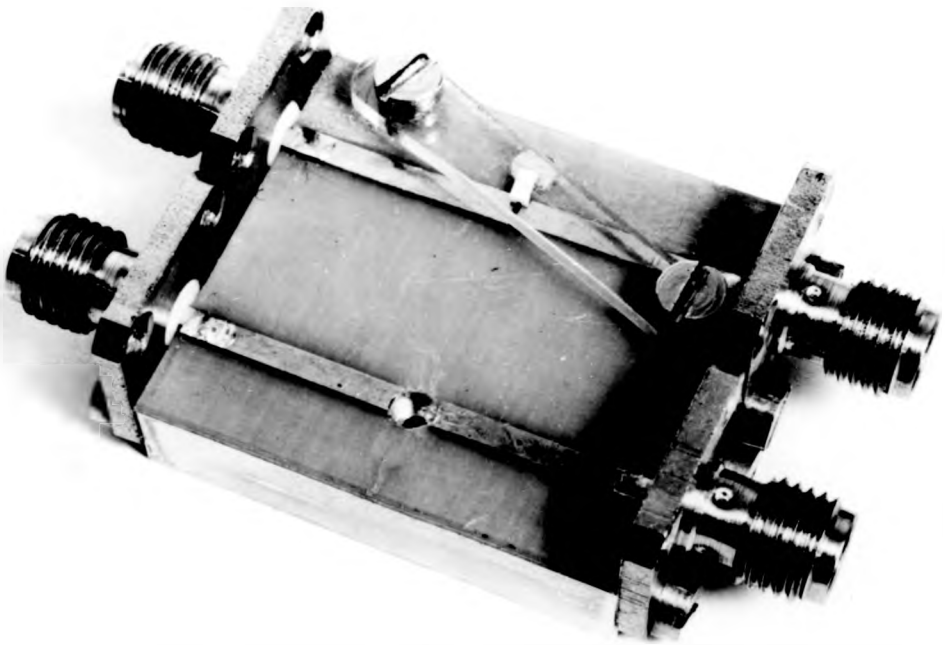


FIG. 4.3. Polyguide test fixture for the comparison of LID and P103 packages.

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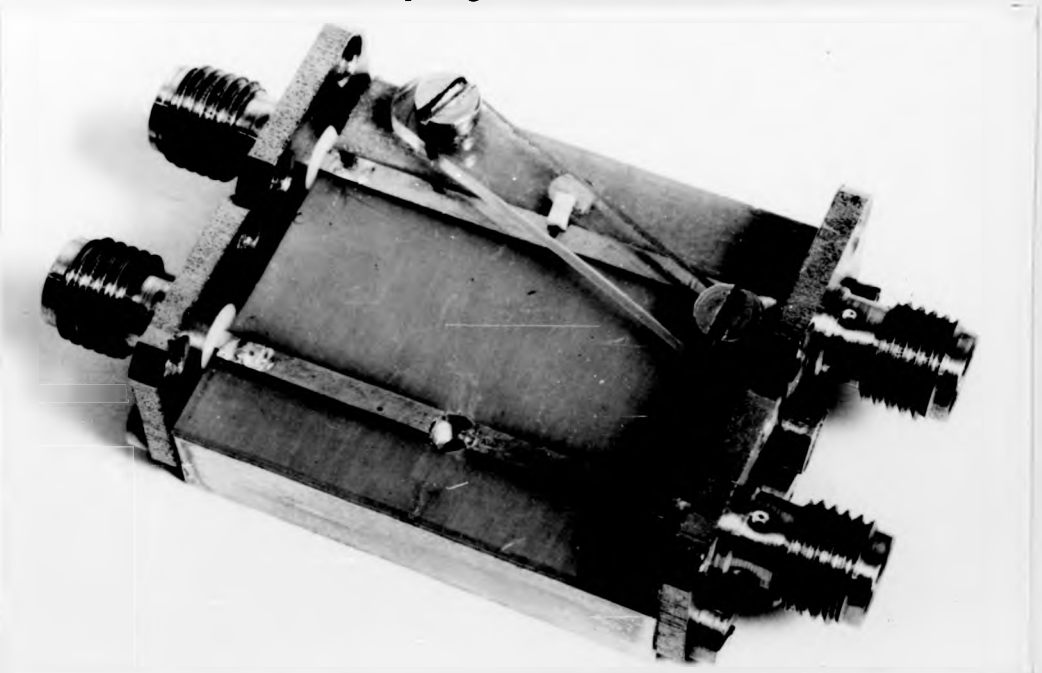

FIG. 4.3. Polyguide test fixture for the comparison of LID and P103 packages.

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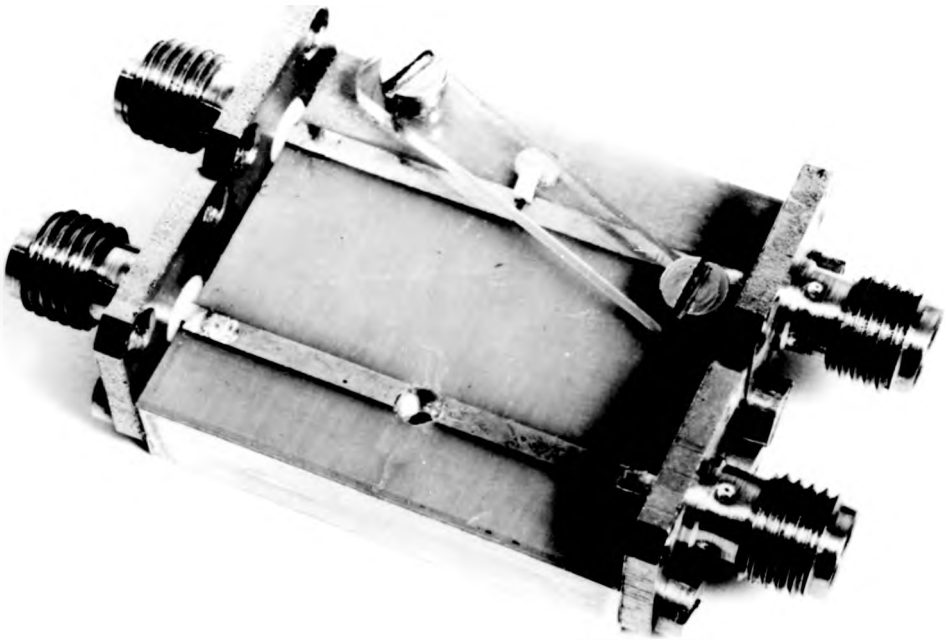


FIG. 4.3. Polyguide test fixture for the comparison of LID and P103 packages.

CHAPTER V.

Characterisation of LID packaged GaAs FETs.

CHAPTER V.

CHARACTERISATION OF LID PACKAGED GaAs FETs.

In applying computer correction to LID packaged devices it was first necessary to optimise the test mount and then realise a suitable calibration process. Having done this FETs of different types were characterised and information on relative performance and parameter spreads fed back to the manufacturer to enable devices and processes to be improved.

5.1. Test Mount Optimisation

As described in Chapter IV alternative substrate configurations were considered for use in the LID mount. The direct source grounding method, via a ground plane pedestal, was finally adopted and the performance optimised with this structure. In order to minimise coupling between the input and output microstrip lines their ends are chamfered where connection is made to the gate and drain pads of the LID package. With a through shim of identical width to the microstrip line in the mount the microstrip to co-axial transitions were tuned with the screws provided, for minimum discontinuity as displayed on a Hewlett Packard time domain reflectometer (TDR) system. The through performance of the optimised mount is shown Figure 5.1.(a). The effect of discontinuities in the test mount is shown in plot (b) which is the result of using a wire bonded through LID package in place of the shim. Although the TDR gave useful information regarding the test mount its resolution was inadequate for determining the precise electrical lengths needed for the calibration procedure.
These were subsequently determined by precise VSWR measurements using a slotted line and a 3GHz microwave source phase locked to a crystal oscillator to ensure frequency stability.

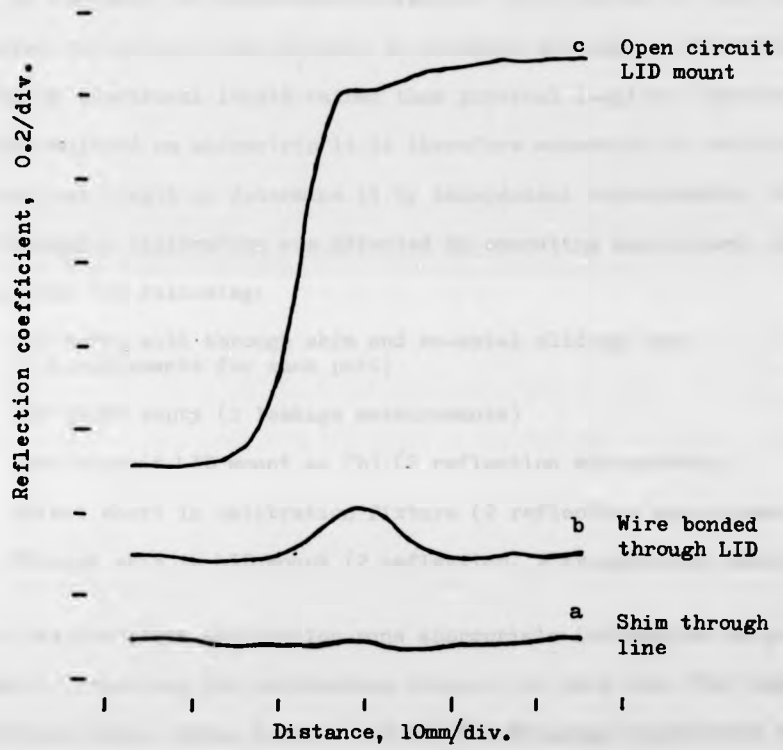


Fig: 5.1. TDR plots of LID test mount, empty and with through devices.

5.2. System Calibration with LID Transistor Fixture

The calibration process utilises options included in the correction programme specifically for such test assemblies where a finite length of through line is needed and open as well as short circuit terminations may be required for calibration purposes. (15). In order to keep the programme general microstrip lines as well as co-axial systems are described in terms of electrical length rather than physical lengths. Where offsets are being realised on microstrip it is therefore necessary to calculate the electrical length or determine it by independent measurements. With the LID fixture, calibration was affected by executing measurement runs having connected the following:

a) LID mount with through shim and co-axial sliding load. (3 measurements for each port)

b) LID mount empty (2 leakage measurements)

c) Open circuit LID mount as (b). (2 reflection measurements)

d) Offset short in calibration fixture (2 reflection measurements)

e) Through shim in LID mount (2 reflection, 2 transmission measurements).

Prior to the above calibration runs appropriate information is given to the computer regarding the calibration pieces. In this case the 'open circuit' reference plane option is selected and the fringing capacitance value (0.03pF) keyed in.

The relative offset length (-2.3mm) of the short circuit in a similar fixture to the LID assembly is also entered. The length of the through connection in the LID mount is small and usually neglected. This was done to allow ready comparison between LID devices measured before and after the option was added to the programme. The small systematic error which results is considered acceptable in most cases. If required this error may be eliminated by recalling test data stored on magnetic tape and recalculating the results including the effective length of the through line.

Following the calibration runs the LID mount with the through connection is normally measured as the first 'device under test' to check that everything is functioning correctly and to enable measurement consistency between runs to be monitored. Having removed the through shim LID packaged GaAs FETs may be carefully positioned in the mount, biased as required and measured. The device parameters may then be dumped on magnetic tape or a print out of the S-parameters and calculated gain performance obtained from the computer, via a line printer.

5.3. LID Packaged Transistor Test Results

During the course of this research programme several tens of LID devices were characterised using the test fixtures and computer corrected measurement facility described. Not all the data obtained will be presented, but only examples to illustrate the reasons for making such measurements and the results obtained. Such measurements are made to satisfy the following requirements:

a) Determine device S-parameters versus frequency and other conditions.

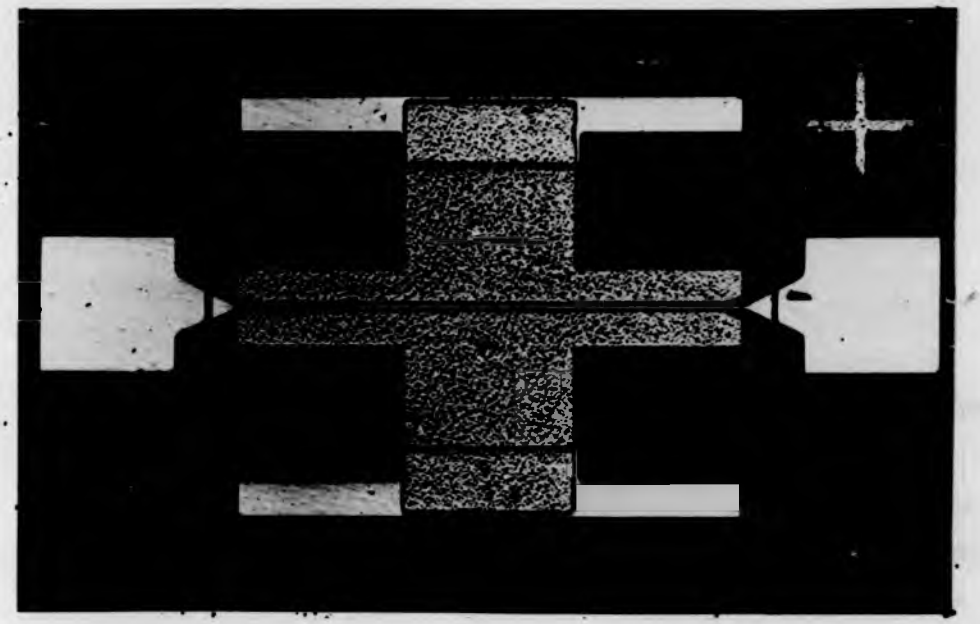
b) Enable amplifier performance to be assessed from S-parameter predictions.

c) To compare performance when developing new devices and processes.

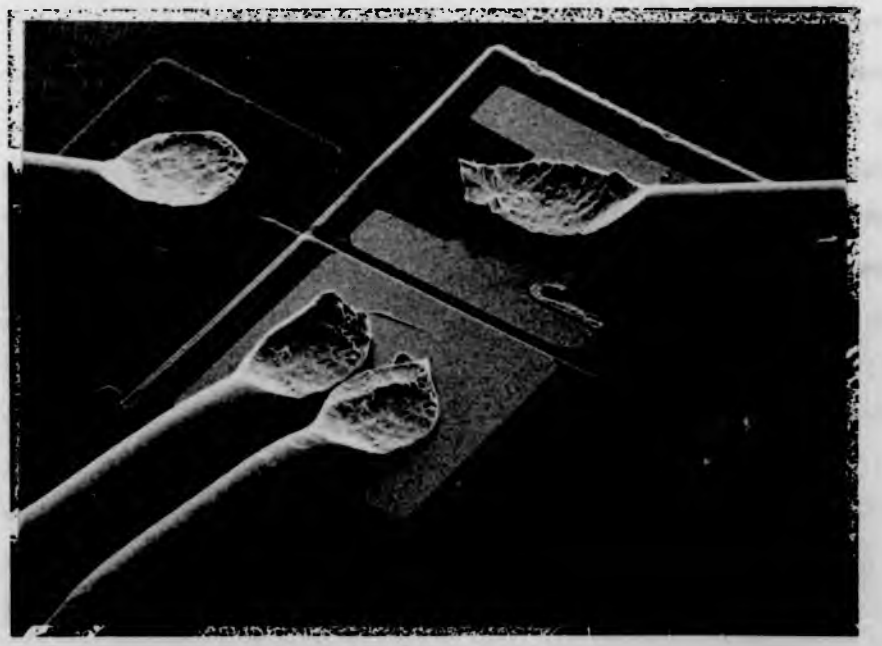
d) To determine parameter spreads and device consistency.

e) Obtain data required for subsequent application of the devices.

Most measurements have been made on two types of Gallium Arsenide FET having gate lengths of 2μm and 1 μm. These devices have similar geometries to the devices subsequently offered commercially by the Plessey Company and designated the GAT 2 and GAT 3 respectively. Fig. 5.2.
In addition to the gate length the GAT 2 and GAT 3 differ in gate width and in the technique used to define the Schottky barrier gate contacts. These differences can be summarised as follows:

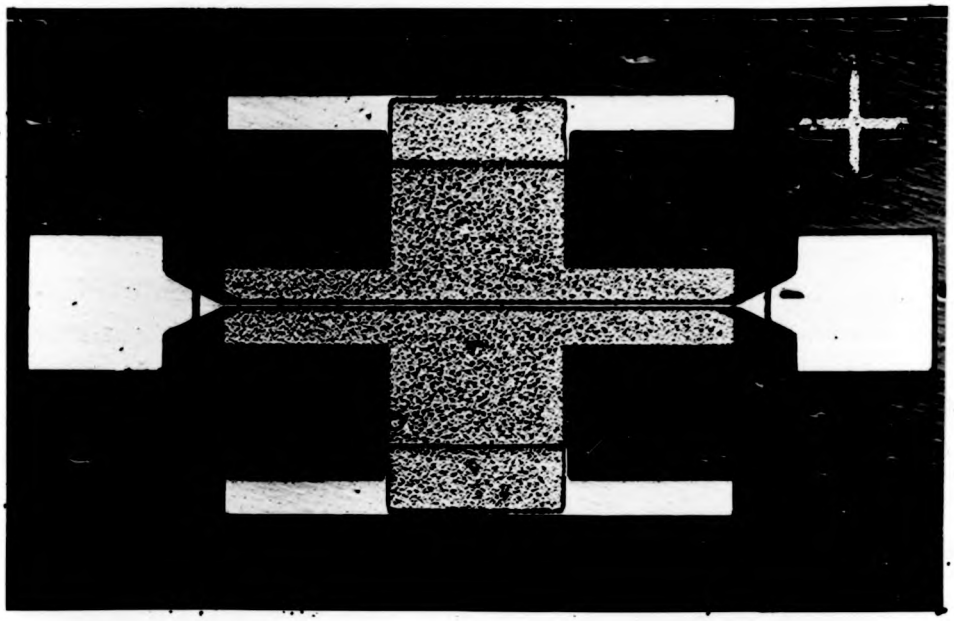


GAT 2 DEVICE CHIP

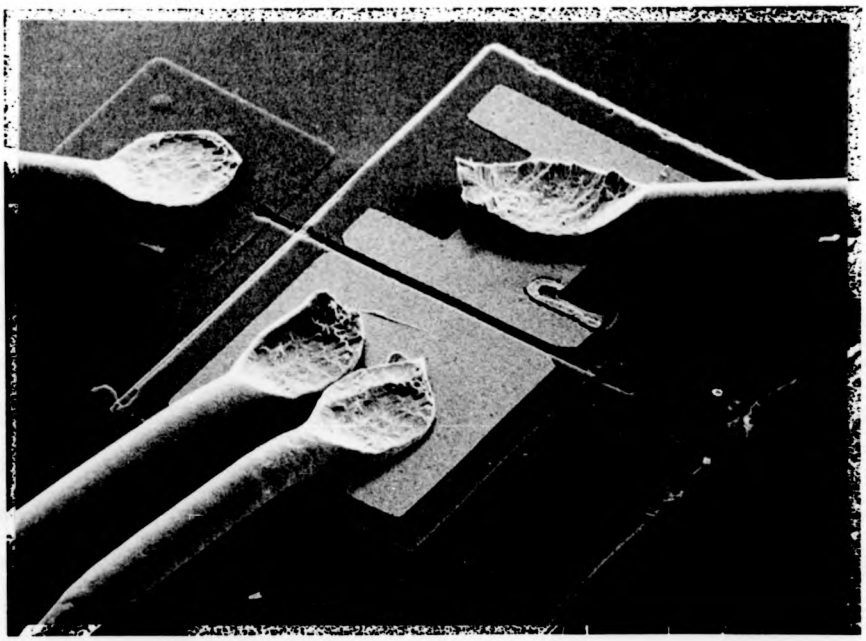


GAT 3 DEVICE CHIP

Fig. 5.2. Photographs showing GaAs FET contact geometries.



GAT 2 DEVICE CHIP



GAT 3 DEVICE CHIP

Fig. 5.2. Photographs showing GaAs FET contact geometries.

Device number	GAT 2	GAT 3
Gate length (nominal)	2 microns	1 micron
Gate Width	360 microns	120 microns
Gate defined using	Photolithography	Electron beam
Useful to	$\sim$6 GHz	$\sim$12 GHz

The technology of GAT 3 devices is complicated by the use of electron beam exposure of a suitable photoresist coating to achieve the micron gate geometry necessary for achieving operation through X-band frequencies.(5) The same metallisation schemes are used for both the GAT 2 and GAT 3. Since the GAT 2 is somewhat easier to manufacture with higher yields this device has been used to assess and optimise modifications to the fabrication procedure while measurements on the GAT 3 have been aimed at determining and improving the high frequency performance of GaAs FETs.

A typical set of broadband, 1.0 GHz to 10 GHz S-parameter results for a LID packaged GAT 3 device are shown in Figure 5.3. The input and output impedances S_{11} and S_{22}, at low frequencies are high and decrease as the frequency rises, particularly the input impedance which at 10GHz approaches the characteristic impedance (50 ohms) of the measurement system. The forward transmission S_{21} of the FET, although changing in phase, remains almost constant in amplitude (unlike a bipolar RF transistor). The peak in the S_{21} for LID packaged devices is due to the influence of the bond wires used to connect the device chip to the package. The reverse isolation S_{12} for this device increases steadily with frequency upto 8GHz and then climbs much faster, again due to parasitic effects associated with the LID package and its bonding. Because these parasitic effects dominate at higher frequencies the LID package has generally been restricted to device assessment and applications below 8 GHz.

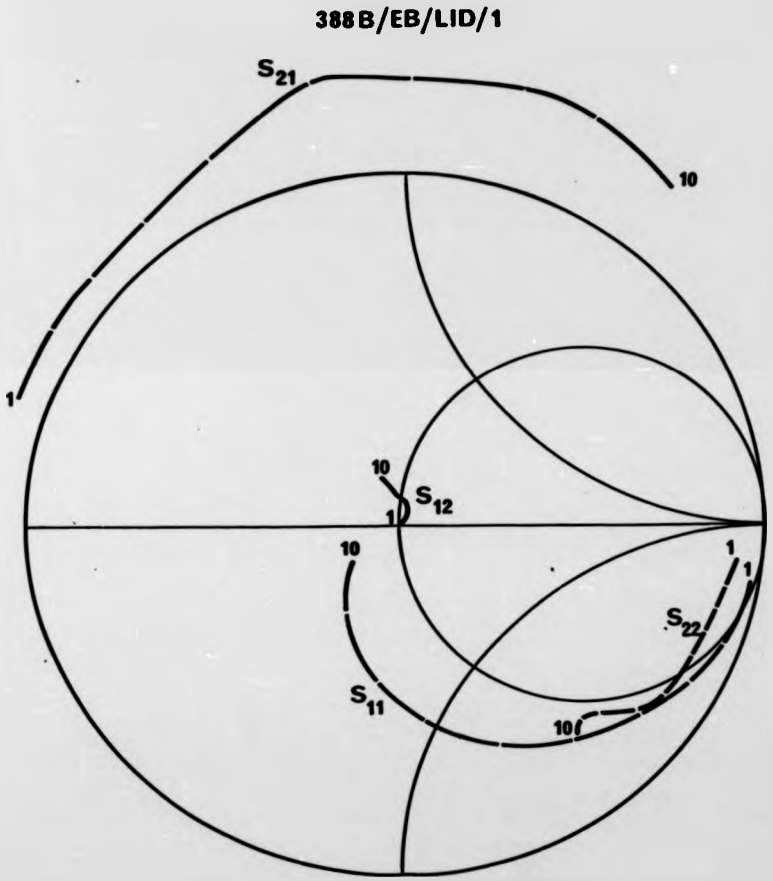


Fig. 5.3. Broadband S-parameters for LID packaged GaAs FET (GAT3)

In order to obtain the above data and Smith plot (Fig.5.3)four separate runs of the computer corrected network analyser were required. The corrected results from each run, Tables 5.1 to 5.4 also show the gain and stability parameters for the device as a function of frequency yielded by this measurement system. The gain parameters enable ready assessment of the amplifier performance of a device and hence facilitate the comparison of devices manufactured in different ways.

5.4. Comparison of Different Device Types

Data shown in Table 5.5 is typical of the comparitive information obtained on numerous device batches using the computer corrected measurement system. In this case the results are for two batches of GAT 2 and GAT 3 devices. Where a reasonable number of devices have been assessed the Standard Deviation, as well as the mean values of the scattering, gain and current parameters is shown, to give an indication of the variation in performance between devices.

Line (1) is the result of 4GHz measurements on a typical aluminium gate GAT 2 batch (417A) and shows S-parameters of the expected amplitude and phase with a predicted gain of about 9dB. This is followed in line (2) by results for devices (Batch 419A) of identical geometry, but having nickel gate contacts. The S-parameters for these devices show considerable differences in both amplitude and phase compared with (1) and have significantly lower gains of around 5.5dB. The interest in nickel gates and the above measurements was an attempt to increase the RF burnout resistance of the GaAs FET. It had been shown that using metals such as nickel in place of aluminium in Schottky barrier mixer diodes burnout characteristics were improved.. (16) Since the failure mechanism for the Schottky gate of the FET was believed to be similar an equal improvement was hoped for. 'Spike' overload measurements on single stage amplifiers did in fact show an improvement in burnout resistance however other amplifier measurements also confirmed the lower gain of the nickel gate devices. The noise figure of these devices was also found to be degraded.

388B/ER/LID/1 5V 0V I(DS)=35 MA.

FREQUENCY GHZ	S11 AMP	S11 PHASE	S12 AMP	S12 PHASE	S21 AMP	S21 PHASE	S22 AMP	S22 PHASE
.400	1.026	-3.5	.015	51.7	1.081	179.4	.905	-.5
.500	.985	-4.9	.031	85.7	1.055	166.8	.909	-5.2
.600	.987	-5.8	.025	82.1	1.122	171.0	.938	-4.2
.700	.993	-5.8	.021	72.0	.961	169.1	.927	-3.6
.800	.986	-7.8	.024	69.6	1.089	168.2	.930	-4.0
.900	.966	-8.8	.022	73.1	1.106	166.0	.956	-3.8
1.000	.968	-9.3	.026	72.9	1.086	163.5	.920	-5.4
1.100	.969	-11.2	.029	74.2	1.093	161.6	.920	-5.8
1.200	.958	-12.0	.029	72.8	1.111	159.6	.930	-5.9
1.300	.962	-12.5	.029	74.2	1.098	158.7	.925	-6.4
1.400	.911	-14.1	.033	72.5	1.167	158.9	.980	-6.5
1.500	.955	-13.2	.034	73.2	1.113	156.6	.933	-7.7
1.600	.963	-14.2	.034	73.3	1.089	155.5	.925	-8.1
1.700	.985	-14.1	.090	57.2	.938	159.1	.923	-8.1

FORTRAN RUN-TIME ERROR IN '9CABS ' CALLED AT LOC X'035D0'.
MAGNITUDE OF ARGUMENT TOO LARGE, OVERFLOW; RESULT = MAXIMUM.

1.800	########	.0	########	-45.0	########	118.9	########	69.3
1.900	.949	-18.4	.042	71.2	1.084	152.9	.920	-9.9
2.000	.935	-19.3	.042	71.8	1.073	151.4	.916	-10.0

FREQUENCY GHZ	MSG DB	K	U DB	MAG DB	CENTRE ON INPUT AMP	CENTRE ON INPUT PHASE	RADIUS	CENTRE ON OUTPUT AMP	CENTRE ON OUTPUT PHASE	RADIUS
.400	18.666	.245	20.973	########	1.026	7.3	.092	.970	-12.9	-.267
.500	15.292	.212	23.233	########	1.063	14.9	.206	2.405	59.0	1.985
.600	16.513	.180	26.064	########	1.076	18.6	.255	2.190	56.9	1.777
.700	16.612	.364	26.946	########	1.069	13.3	.160	14.034	-103.0	-14.367
.800	16.630	.403	25.113	########	1.109	17.9	.224	4.687	59.9	4.194
.900	17.049	.424	23.217	########	1.202	24.8	.366	1.303	24.9	.513
1.000	16.212	.472	20.919	########	1.123	19.3	.223	1.539	33.4	.789
1.100	15.823	.430	21.071	########	1.128	22.3	.246	1.631	37.6	.928
1.200	15.814	.489	20.448	########	1.186	25.5	.315	1.420	29.5	.632
1.300	15.708	.461	20.468	########	1.158	24.9	.283	1.475	32.8	.718
1.400	15.419	.381	23.071	########	4.537	70.7	4.061	1.135	18.7	.278
1.500	15.171	.464	20.390	########	1.236	29.7	.398	1.478	33.6	.718
1.600	15.058	.448	20.575	########	1.187	28.4	.332	1.662	39.6	.953
1.700	10.201	.545	22.936	########	2.197	46.2	1.486	1.177	-69.6	-1.371

FORTRAN RUN-TIME ERROR IN '9CABS ' CALLED AT LOC X'03418'.
MAGNITUDE OF ARGUMENT TOO LARGE, OVERFLOW; RESULT = MAXIMUM.

FORTRAN RUN-TIME ERROR IN '9CABS ' CALLED AT LOC X'0343C'.
MAGNITUDE OF ARGUMENT TOO LARGE, OVERFLOW; RESULT = MAXIMUM.

1.800	-1.479	-1.000	.000	########	.000	.0	########	.000	.0	########
1.900	14.080	.452	18.888	########	1.240	35.2	.409	1.539	38.0	.802
2.000	14.073	.505	17.546	########	1.242	35.2	.388	1.374	31.4	.564

Table: 5.1. Scattering and gain parameters 0.4 to 2.0GHz.

3888/EB/LID/1 5V 0V IIDS1=35 MA.

FREQUENCY GHZ	S11 AMP	S11 PHASE	S12 AMP	S12 PHASE	S21 AMP	S21 PHASE	S22 AMP	S22 PHASE
2.000	.941	-20.3	.038	72.5	1.100	150.8	.906	-10.6
2.100	.938	-21.4	.038	70.3	1.105	149.6	.903	-11.0
2.200	.930	-22.4	.039	70.6	1.100	147.9	.901	-11.2
2.300	.924	-23.3	.039	67.7	1.101	146.4	.901	-11.7
2.400	.918	-24.2	.038	66.6	1.094	145.3	.906	-12.1
2.500	.912	-25.0	.040	68.5	1.086	144.5	.906	-12.7
2.600	.911	-25.6	.041	68.9	1.081	143.9	.909	-13.3
2.700	.910	-26.5	.043	68.5	1.073	142.8	.905	-13.9
2.800	.912	-27.5	.044	68.8	1.067	142.6	.903	-14.5
2.900	.907	-28.6	.044	67.8	1.064	142.5	.898	-15.0
3.000	.902	-29.9	.047	68.5	1.088	141.3	.891	-15.4
3.100	.898	-30.4	.046	66.8	1.094	139.7	.890	-15.6
3.200	.891	-31.7	.050	67.6	1.091	138.2	.884	-16.0
3.300	.881	-32.9	.049	64.8	1.083	137.0	.879	-16.7
3.400	.868	-34.3	.049	64.6	1.111	135.5	.873	-17.2
3.500	.861	-35.1	.050	66.6	1.106	133.7	.872	-17.5
3.600	.852	-36.1	.051	66.8	1.095	131.8	.871	-17.8
3.700	.845	-36.4	.051	65.5	1.095	131.7	.873	-18.2
3.800	.845	-37.8	.051	65.1	1.101	131.1	.873	-18.5
3.900	.845	-38.8	.051	67.4	1.101	129.7	.877	-19.2
4.000	.842	-39.8	.053	64.2	1.096	129.6	.878	-19.7

FREQUENCY GHZ	MAG DB	K	U DB	MAG DB	CENTRE ON INPUT AMP	CENTRE ON INPUT PHASE	RADIUS	CENTRE ON OUTPUT AMP	CENTRE ON OUTPUT PHASE	RADIUS
2.000	14.646	.496	17.760	########	1.180	33.2	.303	1.377	32.8	.573
2.100	14.677	.545	17.415	########	1.189	33.8	.298	1.386	32.1	.558
2.200	14.505	.573	16.805	########	1.204	35.2	.309	1.353	30.5	.503
2.300	14.547	.640	16.473	########	1.229	35.9	.319	1.348	29.1	.468
2.400	14.580	.669	16.264	########	1.250	37.3	.336	1.311	27.6	.411
2.500	14.224	.639	15.954	########	1.257	39.0	.355	1.283	27.8	.388
2.600	14.239	.621	15.934	########	1.262	40.2	.368	1.270	28.2	.378
2.700	13.983	.618	15.707	########	1.265	41.2	.373	1.287	29.5	.401
2.800	13.826	.587	15.647	########	1.250	42.2	.365	1.291	31.0	.418
2.900	13.793	.612	15.173	########	1.242	42.5	.346	1.282	30.7	.397
3.000	13.686	.611	14.896	########	1.246	44.0	.352	1.290	31.4	.408
3.100	13.746	.662	14.753	########	1.268	44.3	.360	1.300	30.9	.400
3.200	13.354	.661	14.214	########	1.282	46.2	.378	1.308	31.5	.410
3.300	13.428	.754	13.607	########	1.293	46.3	.360	1.302	30.5	.370
3.400	13.521	.801	13.238	########	1.312	47.7	.366	1.294	29.9	.347
3.500	13.449	.811	12.943	########	1.316	48.5	.368	1.280	29.6	.327
3.600	13.307	.840	12.592	########	1.336	49.8	.381	1.273	29.3	.312
3.700	13.314	.867	12.462	########	1.357	50.4	.395	1.266	29.1	.297
3.800	13.327	.852	12.522	########	1.355	51.9	.397	1.264	29.5	.298
3.900	13.318	.800	12.659	########	1.345	53.5	.403	1.244	30.2	.290
4.000	13.180	.815	12.582	########	1.374	55.1	.431	1.252	30.7	.295

Table 5.2. Scattering and gain parameters 2.0 to 4.0GHz

3888/EB/LID/1 5V 0V I(DS)=35 MA.

FREQUENCY	S11		S12		S21		S22	
GHZ	AMP	PHASE	AMP	PHASE	AMP	PHASE	AMP	PHASE
4.000	.840	-39.9	.052	65.6	1.102	130.2	.881	-20.2
4.200	.829	-43.5	.055	65.5	1.149	125.5	.879	-22.2
4.400	.810	-47.0	.057	63.9	1.151	125.2	.853	-22.9
4.600	.786	-49.1	.052	66.4	1.184	121.2	.851	-23.4
4.800	.773	-50.7	.053	69.2	1.152	119.6	.862	-24.0
5.000	.765	-52.6	.056	68.9	1.156	117.0	.871	-25.0
5.200	.742	-55.7	.058	70.6	1.210	115.0	.864	-27.0
5.400	.733	-60.5	.062	68.4	1.212	110.9	.849	-28.7
5.600	.716	-64.7	.062	69.5	1.286	109.9	.843	-30.3
5.800	.698	-67.0	.063	76.3	1.284	105.4	.852	-31.4
6.000	.663	-69.2	.068	78.0	1.282	103.1	.855	-32.7
6.200	.632	-74.2	.070	74.5	1.287	99.7	.841	-33.8
6.400	.589	-78.4	.069	73.4	1.296	95.0	.814	-35.3
6.600	.576	-81.0	.074	76.6	1.281	93.5	.801	-36.3
6.800	.570	-85.6	.072	71.2	1.339	91.2	.805	-37.6
7.000	.533	-87.8	.073	76.5	1.270	88.7	.819	-39.3
7.200	.484	-92.0	.069	73.2	1.310	86.7	.804	-40.1
7.400	.444	-97.2	.066	77.7	1.290	81.4	.776	-40.5
7.600	.424	-101.0	.068	78.4	1.276	78.4	.754	-41.0
7.800	.428	-105.8	.068	80.3	1.305	77.7	.757	-42.0
8.000	.396	-105.2	.069	89.7	1.309	74.4	.774	-43.6

FREQUENCY	MSG	K	U	MAG	CENTRE ON INPUT		RADIUS	CENTRE ON OUTPUT		RADIUS
GHZ	DB		DB	DB	AMP	PHASE		AMP	PHASE	
4.000	13.241	.782	12.641	########	1.361	55.5	.428	1.233	31.0	.282
4.200	13.217	.762	12.697	########	1.404	60.6	.483	1.236	33.1	.290
4.400	13.090	.884	11.507	########	1.380	61.5	.414	1.258	33.2	.284
4.600	13.537	.996	11.234	########	1.406	63.1	.407	1.240	32.0	.241
4.800	13.362	.950	11.083	########	1.420	66.0	.436	1.205	31.9	.214
5.000	13.119	.878	11.242	########	1.470	70.1	.512	1.195	32.9	.217
5.200	13.163	.859	11.097	########	1.487	73.9	.537	1.190	34.7	.216
5.400	12.882	.909	10.549	########	1.499	78.0	.531	1.216	36.8	.233
5.600	13.189	.880	10.705	########	1.490	82.2	.532	1.206	38.1	.229
5.800	13.062	.803	10.678	########	1.492	85.5	.565	1.178	38.5	.213
6.000	12.755	.784	10.360	########	1.566	89.6	.654	1.168	39.2	.205
6.200	12.651	.914	9.724	########	1.660	94.4	.696	1.191	39.9	.206
6.400	12.753	1.181	8.816	10.174	1.775	96.7	.702	1.231	40.7	.201
6.600	12.398	1.180	8.347	9.826	1.765	98.4	.693	1.243	41.7	.212
6.800	12.692	1.158	8.773	10.279	1.815	104.2	.748	1.241	43.0	.214
7.000	12.424	1.155	8.358	10.035	1.866	106.7	.798	1.208	43.6	.184
7.200	12.761	1.388	8.023	9.050	2.077	110.9	.901	1.234	43.8	.177
7.400	12.921	1.764	7.177	7.847	2.198	113.1	.871	1.274	43.5	.169
7.600	12.749	1.938	6.624	7.188	2.292	115.9	.892	1.312	43.9	.178
7.800	12.819	1.817	6.884	7.591	2.201	119.6	.856	1.299	44.7	.180
8.000	12.799	1.715	7.050	7.874	2.299	119.1	.973	1.267	45.8	.168

Table 5.3. Scattering and gain parameters 4.0 to 8.0GHz

3888/EB/LID/1 5V 0V IIDSI=38 MA.

FREQUENCY GHZ	S11 AMP	S11 PHASE	S12 AMP	S12 PHASE	S21 AMP	S21 PHASE	S22 AMP	S22 PHASE
8.000	.402	-104.0	.069	88.8	1.288	71.8	.756	-45.3
8.200	.354	-111.4	.071	79.2	1.265	68.0	.736	-46.6
8.400	.309	-121.2	.069	90.1	1.264	65.8	.739	-44.6
8.600	.296	-125.0	.078	98.5	1.253	62.3	.749	-43.7
8.800	.295	-123.5	.086	95.4	1.257	61.1	.751	-45.1
9.000	.275	-123.2	.088	97.2	1.273	62.1	.741	-49.2
9.200	.246	-132.8	.092	95.0	1.228	55.7	.714	-50.6
9.400	.227	-154.0	.092	100.8	1.229	56.5	.711	-49.6
9.600	.205	-164.4	.098	107.3	1.217	49.7	.722	-46.2
9.800	.180	-156.4	.115	108.0	1.208	49.7	.756	-47.6
10.000	.154	-141.2	.131	107.5	1.213	49.0	.765	-51.9
10.200	.136	-144.7	.140	103.3	1.191	50.5	.745	-60.2
10.400	.201	-167.2	.132	101.3	1.195	45.1	.708	-59.8
10.600	.211	168.3	.141	113.2	1.201	44.2	.714	-58.2
10.800	.203	166.9	.159	110.9	1.198	38.6	.730	-54.7
11.000	.120	172.7	.182	114.7	1.171	40.0	.745	-59.3
11.200	.071	-179.2	.211	111.6	1.195	41.0	.805	-66.8
11.400	.121	154.6	.190	112.8	1.113	39.1	.729	-71.0
11.600	.238	136.5	.303	115.8	1.230	40.6	.729	-66.6
11.800	.246	143.5	.284	99.6	1.312	32.4	.780	-61.6
12.000	.163	141.3	.302	100.9	1.340	27.9	.812	-65.9

FREQUENCY GHZ	MSG DB	K	U DB	MAG DB	CENTRE ON INPUT AMP	CENTRE ON INPUT PHASE	RADIUS	CENTRE ON OUTPUT AMP	CENTRE ON OUTPUT PHASE	RADIUS
8.000	12.689	1.858	6.649	7.343	2.306	117.5	.929	1.299	47.7	.176
8.200	12.498	2.120	6.010	6.484	2.719	126.5	1.179	1.345	48.9	.183
8.400	12.605	2.206	5.900	6.402	2.909	133.1	1.305	1.333	46.0	.170
8.600	12.078	1.916	5.933	6.575	2.970	135.9	1.474	1.313	44.9	.180
8.800	11.638	1.712	5.980	6.722	3.059	136.8	1.647	1.313	46.6	.200
9.000	11.687	1.736	5.894	6.608	3.252	134.5	1.812	1.331	50.4	.210
9.200	11.260	1.542	5.146	5.690	3.725	143.1	2.138	1.387	51.6	.225
9.400	11.278	1.580	5.074	5.607	3.903	153.6	2.281	1.391	49.5	.224
9.600	10.946	1.540	5.087	5.652	4.481	160.9	2.900	1.377	46.0	.229
9.800	10.231	1.430	5.469	6.337	5.591	155.4	4.254	1.323	47.5	.242
10.000	9.650	1.232	5.606	6.744	8.646	148.1	7.443	1.322	52.2	.273
10.200	9.310	1.294	5.119	6.056	12.831	145.6	11.563	1.369	60.2	.302
10.400	9.571	1.488	4.749	5.558	5.405	160.1	4.050	1.421	59.2	.316
10.600	9.302	1.362	4.895	5.710	7.425	166.0	6.121	1.433	56.1	.343
10.800	8.765	1.180	5.064	6.418	7.961	170.8	6.832	1.406	52.9	.367
11.000	8.073	1.066	4.951	6.505	19.143	-24.0	-20.212	1.422	58.0	.403
11.200	7.537	.777	6.102	########	5.711	-35.3	-6.453	1.349	66.0	.417
11.400	7.679	1.164	4.290	5.222	7.577	-26.2	-8.764	1.478	69.2	.429
11.600	6.090	.769	5.345	########	2.881	-21.1	-3.579	1.884	59.3	1.003
11.800	6.643	.557	6.703	########	15.295	-1.8	-15.829	1.516	56.5	.712
12.000	6.473	.534	7.334	########	3.995	-7.7	-4.438	1.535	62.2	.748

Table 5.4. Scattering and gain parameters 8.0 to 12.0GHz

TABLE: 5.5. LID PACKAGED GaAs FET PARAMETERS

DEVICE TYPE	BATCH	SAMPLE NO:	COMMENTS	S_{11} Mag^n	S_{11} Phase	S_{12} Mag^n	S_{12} Phase	S_{21} Mag^n	S_{21} Phase	S_{22} Mag^n	S_{22} Phase	Maximum Available Gain(MAG)	Unilateral Gain (U)	Drain Current I_{ds}
1. GAT 2	417A	6	Mean values, 4GHz	.43	-101.8	.05	72.9	1.26	90.9	.84	-24.5	8.8	8.2	30.8
			Standard deviation	.028	4.8	.009	7.3	099	2.1	.013	.6	1.1	1.0	12.3
2. GAT 2	419A	2	Mean values, 4GHz	.55	- 72.3	.093	57.6	.96	95.9	.80	-31.3	5.6	5.5	16.5
3. GAT 3	390C	8	Mean values, 4GHz	.87	- 36.9	.063	65.1	.78	128.9	.90	-19.5	-	11.1	38.1
			Standard deviation	.036	4.0	.005	2.3	.15	4.2	.005	.5		1.6	13.6
4. "	"	"	Mean @ 4GHz, I_{DS}=20mA	.86	- 34.6	.064	66.2	.69	131.6	.85	-19.8	-	-	20
			Standard deviation	.025	3.2	.006	1.8	.11	3.3	.009	.8			0
5. GAT 3	398A	8	Mean values, 4GHz	.88	- 37.5	.065	64.6	.85	130.5	.90	-19.8	-	12.7	39.9
			Standard deviation	.050	5.2	.018	2.3	.19	3.7	.024	1.0		2.1	9.6
6. GAT 3	390C	8	Mean values, 8GHz	.48	- 98.1	.077	81.1	.99	75.1	.81	-45.0	3.9	3.6	38.1
			Standard deviation	.087	13.9	.008	9.9	.15	7.0	.01	1.1	1.0	1.0	13.6
7. "	"	"	Mean @ 8GHz, 20mA	.50	- 89.4	.082	69.5	.89	80.8	.74	-45.8	-	-	20
			Standard deviation	.069	11.6	.013	8.2	.11	4.5	.018	1.9			0
8. GAT 3	398A	8	Mean values 8GHz	.46	-100.2	.082	81.0	1.05	73.3	.80	-45.6	6.7	6.0	39.9
			Standard deviation	.14	14.7	.029	6.3	.17	6.4	.025	3.1	0.6	0.4	9.6

Nickel was finally abandoned in favour of aluminium in order to achieve the highest possible gains and low noise performance. The first set of GAT 3 data, line (3) is for a batch of devices which has a low S_{21} and consequently poorer than average unilateral gain at 4 GHz. Because the GAT 3 device is only conditionally stable at this frequency the maximum available gain is infinity and not a useful parameter. Comparison of the GAT 2 and GAT 3 S-parameters, lines (1) and (3) shows the latter having higher input and output impedances, S_{11} and S_{22}. The reverse transmission S_{12} is greater and the forward transmission S_{21} lower for the GAT 3. These effects are all compatible with the smaller overall geometries of the higher frequency one micron gate length GAT 3 device.

For both the GAT 2 and GAT 3 (or any GaAs FET) the parameter which shows the greatest variation is the saturated drain current, Idss. This arises from the dependance of I_{DSS} on the cube of the channel thickness: $I_{DSS} \propto a^3$ where a = channel thickness. Since a is the order of a micron small variations resulting from uneven epitaxial growth or subsequent etching of the n-type channel layer result in large drain current variations. Fortunately as can be seen spreads in microwave parameters do not follow the large current differences. The variations which do occur can, to some extent, be reduced by operating devices at the same drain current, 20mA in the case of line (4) by applying the appropriate negative gate bias.

Line (5) is the results for a more typical batch (398A) of GAT 3 devices also measured at 4GHz and biassed at I_{DSS}. Comparing with line (3) the S_{21} is higher and the Unilateral Gain better by 1.6dB. The remaining S-parameters show excellent agreement between the two device batches which is consistent with material rather than geometry differences affecting performance. The slightly inferior performance of batch 390C can be related to the lower n carrier mobility of the epitaxial GaAs layer on the wafer used to fabricate these devices.

The consistency of S-parameters shown between batches of devices is remarkable when one considers that the active part of the device is only 4 x 120 microns in area with a 1 micron metal gate stripe deposited in the middle. On the GAT 3 device the electron beam defined gate stripe runs off the mesa area and has an aluminium bonding pad deposited over it. A problem with this process was identified from measurements on two devices from batch 398A, not included in the above results. Initially these devices were thought to have been damaged during bonding since the drain current could not be controlled by gate bias and the S-parameters (Table 5.6) corresponded to a lossy bilateral device, $S_{12} \simeq S_{21}$. Since no physical defects could be found the devices were carefully probe tested. The gate diode characteristic was found to appear only after the application of positive bias such that a forward current flow of about 10mA occurred. This current 'burn-in' fused the gate metallisation to the bonding pad overcoming the initial lack of electrical contact. After this 'burn-in' the devices performed normally both d.c. and RF wise as shown by the S-parameters.

In order to prevent recurrence of this problem changes were subsequently made to the device fabrication process which ensured that an intimate contact was established between the gate and its bonding pad.
Returning to Table5.5 lines (6) to (8) show results for the same GAT 3 devices as lines (3) to(5) but measured at 8GHz. As expected the input and output impedances are lower than at 4GHz. Both the forward and reverse transmissions S_{12} and S_{21} show slight increases, the latter arising from matching effects due to the LID package and associated bond wires.

While the S-parameters at I_{DSS} for both device batches, lines (6) and (8) are still very similar the gain differences for MAG and U are much greater. Devices from batch 398A are obviously more suitable for operation at 8GHz since their predicted gains are almost twice that of devices from batch 390C.

TABLE 5.6.: S-PARAMETERS OF GAT 3 DEVICE WITH POOR GATE CONTACT TO WIRE BOND PAD.

Device No: 398 A/EB/LID/9

Comments	Frequency (GHz)	S_{11}		S_{12}		S_{21}		S_{22}	
		Mag	Phase	Mag	Phase	Mag	Phase	Mag	Phase
Initial testing	4.0	.99	-15.1	.064	70.1	.069	74.8	.90	-19.8
I_{DSS} = 58mA	8.0	.96	-36.2	.132	49.2	.138	50.6	.84	-52.6
After 'burn-in'	4.0	.79	-34.7	.060	73.6	.90	119.7	.92	-21.4
I_{DSS} = 51mA	8.0	.39	-69.4	.089	78.8	.96	68.1	.83	-45.4

This illustrates two important points:

i) Small S-parameter differences significantly affect device amplifier performance.

ii) Calculation of gain parameters as part of a computer corrected measurement system is an important aid to device comparison.

Results similar to those discussed above were obtained for numerous other batches of devices mounted in LID packages. This information was fed back to the device manufacturers and contributed to the optimisation of the fabrication process since effects of process changes could be readily assessed against the resulting FETs performance.

CHAPTER VI.

Parameters of devices in other packages.

CHAPTER VI

PARAMETERS OF DEVICES IN OTHER PACKAGES

6.1. 'Studded' (P103) Package Measurements

As discussed in Chapter IV a pair of microstrip test circuits were produced specially for the characterisation of P103 packaged devices. These are shown in Fig.6.1 and consist of one substrate machined to accept the threaded stud of the P103 packaged device under test and a second with a through 50 ohm line for calibration purposes.

As with the LID devices measurements were made using the 2-port full correction programme and the options included in it for different calibration standards. In this case calibration was effected using the two polyguide microstrip circuits plus a coaxial SMA shortcircuit. Precision VSWR measurements were used to establish the offset length of the short relative to the open circuit reference plane as -2.4mm. Similarly the open circuit capacitance of the empty test jig was determined as 0.02pF. After selecting the 'open circuit' reference plane calibration option and inputting the above data the following calibration measurement runs were executed:

a) Through substrate with co-axial sliding load.
   (3 measurements for each port)
b) Empty P103 test substrate (2 leakage measurements)
c) Open circuit P103 substrate, as (b). (2 reflection measurements)
d) Co-axial (SMA) offset short (1 measurement for each port).
e) Through substrate. (2 reflection, 2 transmission measurements).

After calibration the through substrate was usually measured as the first 'device under test' and the results displayed to check the operation of the system before connecting active devices.

Fig. 6.1. P103 package test substrates.

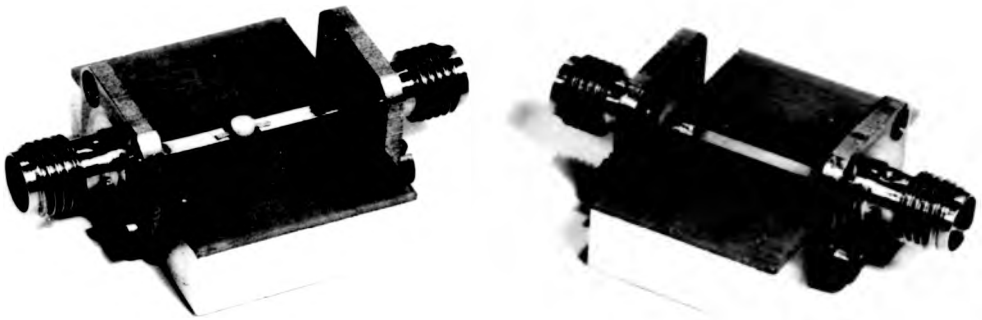


Fig. 6.1. P103 package test substrates.

GaAs FETs in P103 packages to be characterised were inserted into the test substrate and held in position by a nut on the threaded stud. Contact between the package tabs and the transmission lines was maintained by the spring action of the tabs which were bent slightly towards the stud before insertion.

6.2. P103 Packaged Device Test Results

Results for various devices at spot frequencies taken from swept frequency measurements are shown in Table 6.1. The first five sets of data is the result of comparative measurements on experimental devices made during one system run and hence sharing a common set of calibration conditions. This removes any possible effects due to small errors arising from separate calibration and measurement runs being carried out at different times.

The first device (1) is an electron beam defined gate GAT 3 device similar to those characterised in LID packages. Comparison with Table 5.5.(line 3) reveals that S_{11}, S_{12} and S_{22} are very similar to the LID packaged equivalent. Significant differences in phase angles are observed, but these are to be expected due to the larger physical size of the P103 package and hence the positioning of the reference planes. The larger S_{21} and gain parameters of the P103 packaged device at the frequencies shown is only partly due to the package and mainly reflects the better performance of the device chip used.

The following set of data (2) is for a later version of the GAT 3 device, identical in size and geometry, but having a photolithographically defined gate electrode. Improvements in photolithographic and sub micron mask techniques had made this possible, simplifying the processing of high frequency GaAs FETs. The similarity of the S-parameters and gains for both types of device, which was confirmed with other device measurements, established the validity of the photolithographic process.

TABLE 6.1: P103 PACKAGED GaAs FET PARAMETERS

Device type	Batch No.	Frequency (GHz)	S_{11} Mag.	S_{11} Phase	S_{12} Mag.	S_{12} Phase	S_{21} Mag.	S_{21} Phase	S_{22} Mag.	S_{22} Phase	Max.Gain MAG.	Unilateral Gain U.	Current I_{DSS}
1. GAT 3	429R/13	4.0	.87	- 67.4	.077	36.3	1.32	108.5	.91	-34.8		16.4	19.5
		8.0	.51	-156.4	.084	22.4	1.31	25.8	.77	-74.3	8.3	7.6	"
2. GAT 3 (Photolith)	469A/1	4.0	.99	- 52.1	.080	58.3	1.16	119.0	.94	-31.7		37.3	32
		8.0	.59	-140.4	.094	8.1	1.22	37.5	.75	-86.3	7.2	7.9	"
3. GAT 4	500A/5	4.0	.79	- 74.8	.082	36.8	1.70	99.9	.77	-41.4		12.6	37
		8.0	.41	-172.1	.118	31.0	1.50	16.7	.59	-92.7	6.9	6.1	"
4. GAT 4 ($\frac{1}{2}$ micron)	509A/3	4.0	.78	- 63.7	.087	36.9	1.03	99.9	.90	-34.9		11.3	17
		8.0	.35	-144.1	.104	20.8	.98	21.2	.76	-76.2	4.2	4.1	"
5. GAT 5	515A/1	4.0	.56	-125.8	.072	31.4	1.49	72.4	.77	-38.9	9.6	9.0	41
		8.0	.43	113.5	.145	41.8	1.01	-3.2	.65	-89.2	4.5	3.3	"
6. GAT 1	447/7	1.0	.86	- 53.6	.064	51.2	2.12	133.1	.85	-23.1	-	-	31
		2.0	.65	-102.1	.095	23.2	1.66	92.5	.73	-36.5	-	-	"
7. GAT 4	536D/4	1.0	.98	- 21.8	.020	77.0	2.19	157.7	.86	-16.2	-	-	62
		2.0	.91	- 45.6	.038	53.8	2.14	133.3	.81	-27.6	-	-	"

This process was subsequently adopted for the production of GAT 3 devices as well as being used for experimental devices of new geometries. Data for three such devices is shown in lines (3), (4) and (5), all of which were wide (360 microns) gate devices. By increasing the width of the gate it was hoped to produce FETs with lower input and output impedances which would be easier to match in amplifier circuits, especially for broad-band operation.

Results for the first device (3) show that this objective is realised, S_{11} and S_{22} are lower compared with the GAT 3 and S_{12} and S_{21} are increased. The latter increases are also expected for the wide device. The overall gain available from the device both MAG and U have however been degraded. Two ways of recovering the gain were considered, (a) by reducing the gate length and (b) by reducing the ohmic contact (source and drain) resistances through the use of an n+ contact layer.

Characterisation of half micron gate length devices (4) revealed that rather than increasing the gain with a reduction in gate length further degradation had occurred. This effect is due to the increased series resistance associated with the shorter gate length. No attempt had been made to keep the gate strip resistance the same or to minimise it with the result that the losses increased more than the improvement in gain. Considering the gate as a strip of dimension 0.5 x 0.2 x 360μm its series resistance can be calculated from:

$R = pl/A$ where p = specific resistance
l = length
A = cross sectional area

Taking p = 2.62 microhms/cm. cube for aluminium yields: R = 94.3 ohms

Before the importance of the gate resistance was appreciated an initial batch of n+ contact FETs had been produced and a sample assessed (5). The performance of these devices was again poor and the S-parameters varied wildly compared to normal devices (3). In this case the poor performance and S-parameter variations were believed to be due to a processing problem, namely incomplete removal of the n+ layer between the source and drain contacts before the deposition of the gate.

In order to reduce the effect of the gate resistance an alternative geometry having two gate strips of half the total width was investigated. This geometry was adopted for the commercial GAT 4 device and when successfully combined with n+ contact technology gave the commercial GAT5. Fig 6.2

The last two sets of data in table 6.1, (6) and (7) illustrate the low frequency S-parameters of production GAT 1 and the above geometry GAT 4 devices in P103 packages. It can be seen that at frequencies of 2 GHz and below the impedances of the GAT 4 again are very high making matching difficult.

6.3. Relative Performance of Packages Investigated.

The high frequency (>4GHz) performance of various packaged GaAs FETs has been described in chapters V and VI. Lower frequency (1-2GHz) measurements were also carried out to assess the relative performance of the LID and TO-72 package and to obtain S-parameters for subsequent amplifier circuit design. Table 6.2 summarises the measured S-parameters for both types of package when used with FET chips from the same production batch (Batch No. 343C). The greatest difference in the S-parameters measured for these packages occurs in the phase angles. This however, is to be expected due to the dissimilarity of the packages physical dimensions.

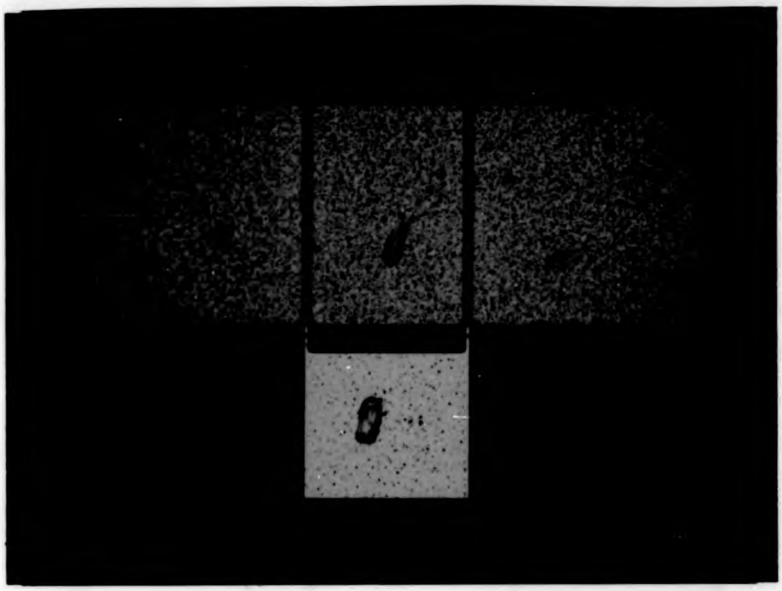


Fig. 6.2. GAT 4/5 Device chip photograph showing contact geometry.

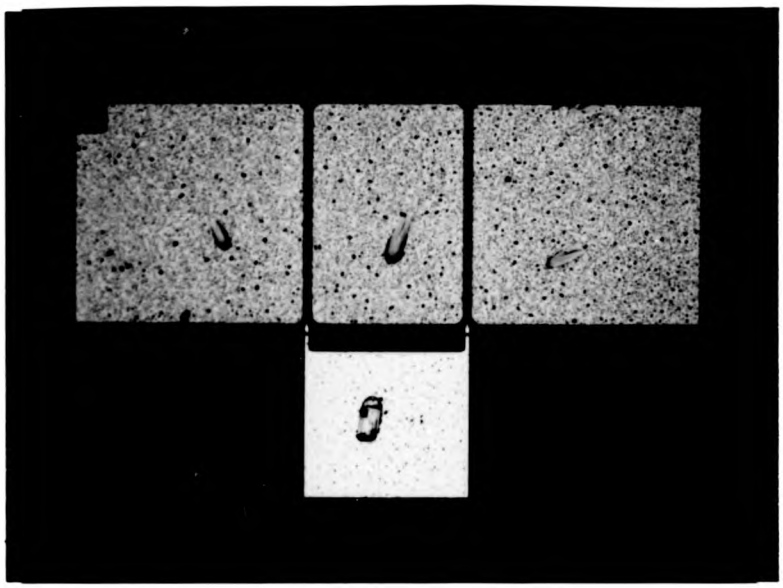


Fig. 6.2. GAT 4/5 Device chip photograph showing contact geometry.

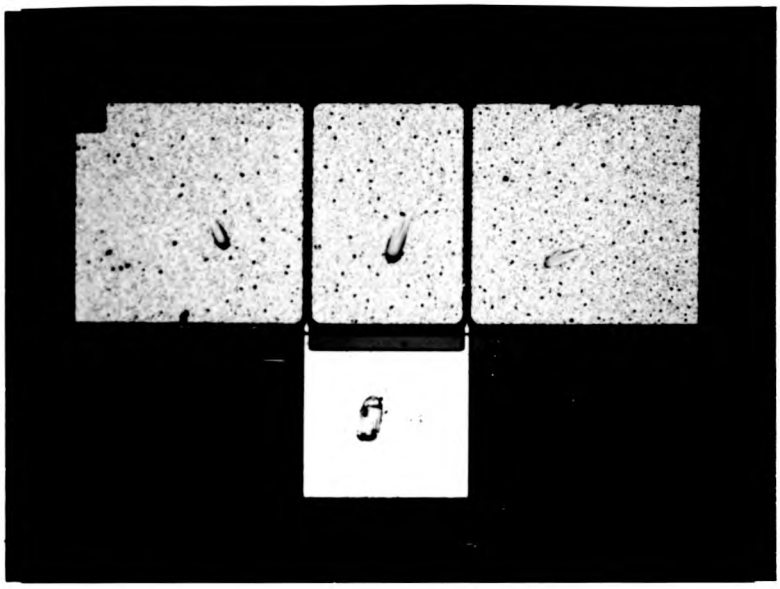


Fig. 6.2. GAT 4/5 Device chip photograph showing contact geometry.

TABLE: 6.2.

S-PARAMETERS OF LID AND TO-72 PACKAGED GAT 1 DEVICES AT I_{DSS} (BATCH 343C)

PACKAGE	FREQUENCY (GHz)	S_{11}	S_{12}	S_{21}	S_{22}
LID	1.0	.87 - 37	.05 61	1.85 141	.86 - 10
"	1.5	.75 - 54	.07 58	1.69 124	.84 - 14
"	2.0	.64 - 71	.08 56	1.59 110	.82 - 18
TO-72	1.0	.73 - 57	.04 66	1.75 104	.85 - 31
"	1.5	.58 - 87	.04 80	1.42 72	.88 - 44
"	2.0	.48 - 98	.05 146	1.08 44	.85 - 57

A more significant variation occurs in S_{21} which exhibits a faster roll-off with frequenoy for the TO-72 than for the LID package. The TO-72 package was not designed for microwave applications and these measurements confirm that its performance, not unexpectedly, degrades above 1GHz.

At 1GHz when used in actual low noise amplifier circuits similar performance is obtained for both LID and TO-72 packaged GAT 1 devices as shown in Table 6.3. If the circuit is tuned for maximum gain however the LID package proves to be superior, as predicted by the S-parameters. In spite of offering some performance improvement, LID packaged devices were seldom used at frequencies as low as 1GHz because of handling difficulties resulting from its small size and having the GaAs FET chip exposed. The LID package was subsequently replaced by the P103 when the ultimate performance was required from GAT 1 devices.

At frequencies above about 10GHz parasitic effects associated with the LID package cause its performance to degrade in a similar manner to the TO-72 package at 2GHz. Since these effects are mainly reactive and can in theory be tuned out the gain parameters calculated from S-parameters still describe the potential performance of the active device. It may not be possible to achieve this performance because the impedances resulting from the package/device interaction prove impossible to match in the appropriate way. In comparing results for the LID with the lower parasitic P103 package it is observed that while similar values are calculated for the maximum available gain (MAG) and unilateral gain (u) the measured values of S_{21} are higher for the P103 package. Since S_{21} is the intrinsic gain of the device in a 50 ohm system, with no matching, the larger this value the less matching is required in an amplifier circuit.

Again the difference in performance was expected since the P103 package was designed as a 12GHz GaAs FET package whereas the LID was not. Unfortunately the P103 package only became available near the end of this study after many comparitive measurements had been made with LID devices.

TABLE:6.3.

AMPLIFIER PERFORMANCE OF LID AND TO-72 PACKAGED GAT 1 DEVICES (BATCH 343C).

CIRCUIT MATCHED FOR:	LID PACKAGE		TO-72 PACKAGE	
	Gain	Noise Figure	Gain	Noise Figure
Minimum Noise Figure:	13dB	2.6 dB	12dB	2.6dB
Maximum Gain (V_{DS} = +5V, V_{GS}= 0V)	18dB	6 dB	12dB	3.5dB

6.4. Microwave Parameters of Chip Devices

Early in this investigation considerable attention was directed at characterising the high frequency GAT 3 devices in chip form. Chip parameters were of interest since they relate the intrinsic characteristics of the active device and are required if the device is to be used in circuits in chip form. The latter is desirable if the ultimate in performance is required especially in broad bandwidth applications where it may be impossible to match a packaged device.

To characterise FET chips requires their installation on a suitable test substrate with the common source terminal grounded and the gate and drain connected to input and output 50 ohm microstrip transmission lines. Alumina substrates 1 inch square and 0.025 inch thick with a gold plated ground plane on one side and photolithographically defined 50 ohm microstrip lines on the other were produced for test and calibration substrates. Devices were mounted on studs fixed into holes drilled in the substrate and the device gate and drain contacts wire bonded to 50 ohm transmission lines on either side of the stud. Source bonds were made to the stud which was in good electrical contact with the ground plane.Fig.6.3(a). This technique became known as the 'COD' mounting or Chip On Disc(17) Various calibration substrates were produced with through lines, reference open circuits and offset open circuits. Early measurements on microstrip short circuits on Alumina substrates showed that it was impracticable to realise a calibration standard short for operation to 12GHz. Open rather than short circuit calibrating terminations were therefore pursued. A test and calibration substrate are shown. Fig.6.3.(b).

Initial measurements made using the two port correction routine and the above test pieces gave erratic results for both FETs and passive devices. Part of the problem was found to be due to shortcomings in the calibrating open circuit lines. A partial solution to this calibration problem was achieved by using one coaxial short as an offset short and a single microstrip open circuit to define the device measurement plane.

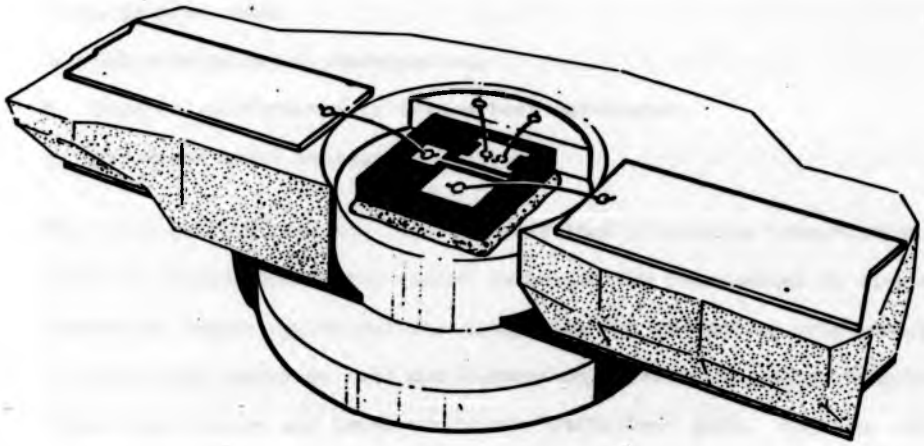


Fig. 6.3(a)COD mounted FET chip on alumina substrate.

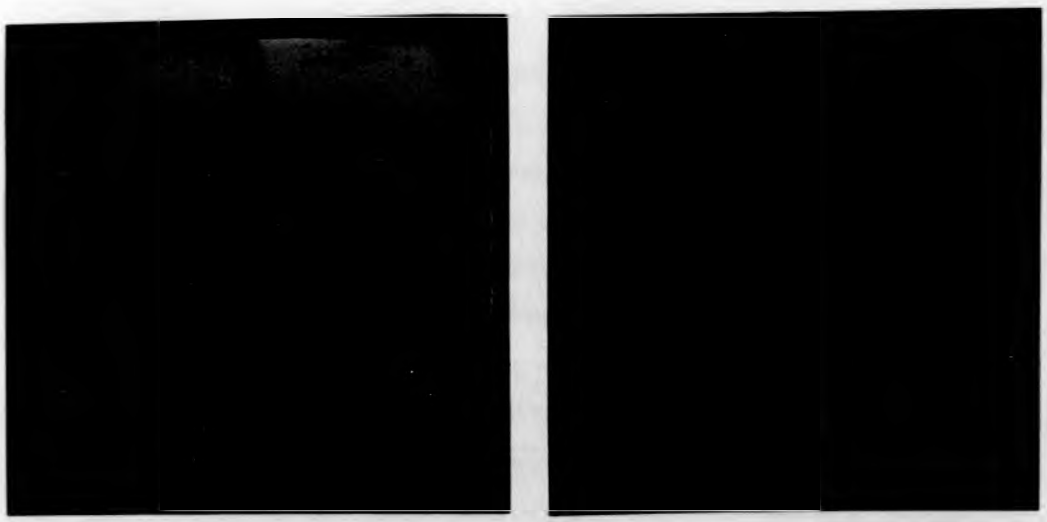


Fig.6.3(b) Alumina test and calibration substrates.

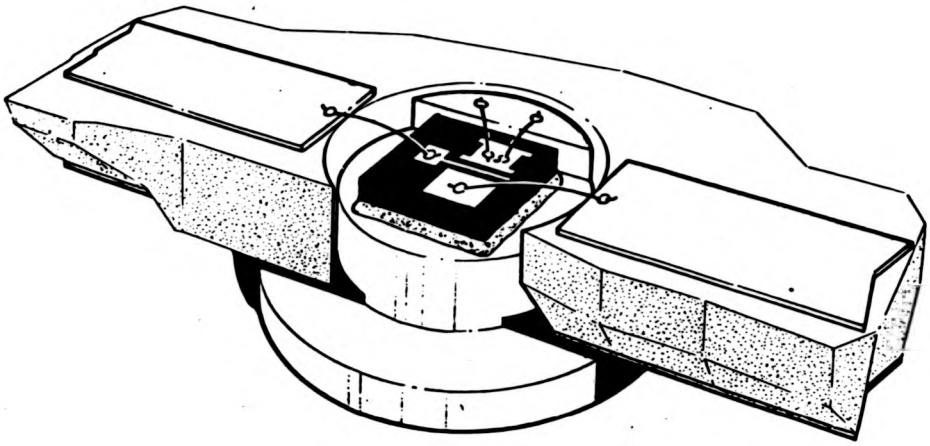


Fig. 6.3(a)COD mounted FET chip on alumina substrate.

Fig.6.3(b) Alumina test and calibration substrates.

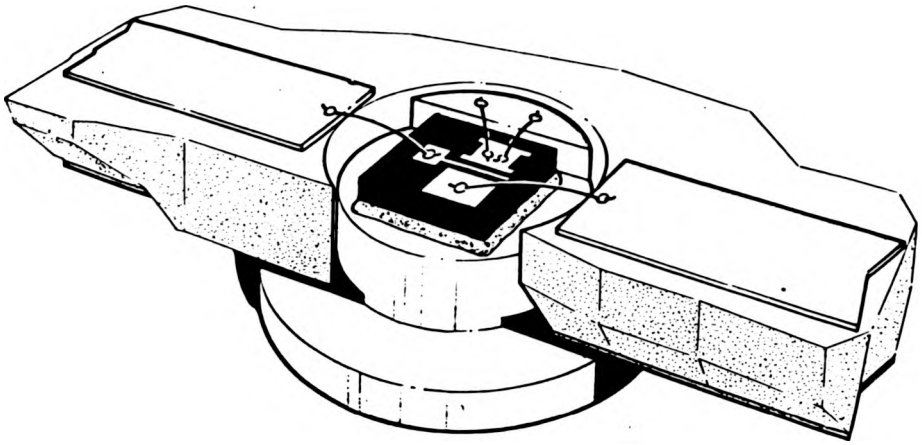


Fig. 6.3(a)COD mounted FET chip on alumina substrate.

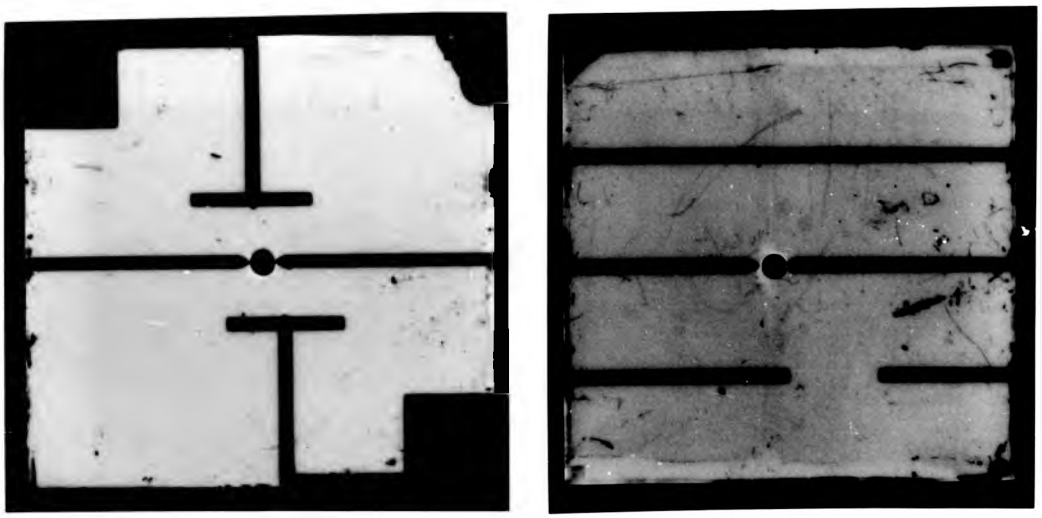


Fig.6.3(b) Alumina test and calibration substrates.

Further measurements with this modified calibration procedure were better, but still gave variable results. Investigation of these effects identified three problem areas:

1. Calibration piece inadequacies.
2. Physical differences in device test substrates.
3. Substrate mount mechanical problems.

The first problem resulted from the fact that microstrip transmission lines on alumina substrates cannot be accurately represented by simple electrical length equivalents as assumed by the correction programme.(18-21).By so doing both radiation loss and dispersion effects are neglected giving calibration errors and hence erronious 'corrected' data. Physical differences in test substrates arose from manufacturing tolerances on the alumina and the accuracy with which the COD holes could be drilled. The latter were produced using ultrasonic drilling and even though a special jig was used it was difficult to position the holes to better than $\pm$ 0.2mm. On alumina substrates mechanical differences of this order give significant phase variations, as discussed in Chapter IV.

Measurements were made with substrates positioned on a one inch square metal block having co-axial to microstrip transitions screwed to its side. To change substrates the transitions could be unscrewed and removed. The performance of the transitions when changing substrates was inconsistent, especially if a substrate was slightly oversize and interfered with the ground continuity between the transition and the mounting block.

While given time the above problems could probably have been overcome this method of characterising GaAs FETs, was finally abandoned. In addition to the difficulties discussed the assessment of chip devices suffered other drawbacks. Since the test was a 'destructive' one, the chips could not be removed from the test substrate and re-used, it was not suited to comparitive studies or determining amplifier performance with known devices. For these measurements and studies packaged devices,(LID and P103) were used which could be returned to the manufacturer or used in circuits following their S-parameter characterisation.

The work with chip devices had two useful outcomes. The first was the discovery of a simple tuning technique to realise high frequency amplifiers, first used to check the predicted gains of chip devices based on their measured S-parameters. This was later applied to multistage units as described in Chapter VII.

As a result of the problems identified by this work in measuring chip parameters other ways of obtaining this information were considered. This subsequently led to the development of successful techniques by colleagues of the author which are now used when chip FET parameters are required. (22)

6.5. Comparison of Measured and Theoretical FET Parameters

The action of a n-channel depletion mode GaAs MESFET can usefully be represented by the simplified equivalent circuit, Fig. 6.4. Parasitic inductance and capacitance associated with the package have been ommitted since at low frequencies their effects are negligible.

The nature of the elements shown and expected values for a 2 micron gate length (GAT 2) devices are:

R_g	-	effective gate resistance	5 ohms
R_s	-	effective source resistance	5 ohms
R_d	-	effective drain resistance	1000 ohms
R_i	-	resistance associated with C_{gs}	5 ohms
C_{gs}	-	effective gate source capacitance	0.5pF
C_{dg}	-	effective drain gate capacitance	0.05pF
C_{ds}	-	effective drain source capacitance	0.1pF
G_{mo}	-	low frequency transconductance	12mmho
τ	-	carrier transit time	5pS

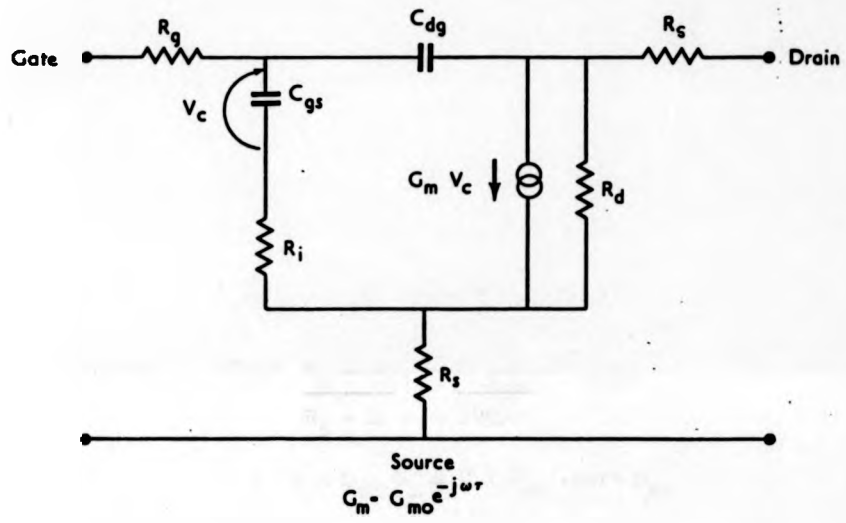


Fig: 6.4 Equivalent circuit of GaAs F.E.T.

This equivalent circuit allows a ready check of S-parameter data at the boundary condition f = OHz and hence establishes reference points with which measured S-parameters can be compared. If these boundary values are not satisfied either the data or the device model is invalid. In the case when the frequency tends to zero from inspection of the equivalent circuit the following S-parameter values would be expected:

S_{11}	= 1, 0°	Effectively an open circuit reflection
S_{12}	= 0, 0°	No reverse transmission, due to open circuit
S_{21}	= G, 180°	50 ohm system gain G, with signal inversion
S_{22}	= T_o 0°	Output conductance T_o

For GAT 2 device: $T_o \simeq \frac{R_d - Z_o}{R_d + Z_o} = \frac{950}{1050} = 0.90$

and gain $G = 2 \times G_{mo} Z_o = 0.1\, G_{mo}$ where G_{mo} is in mmhos

For the GAT 2 example $G \simeq 1.2$

The S-parameters for the GAT 2 example at the low frequency limit of operation, d.c. would therefore be expected to have the values:

$S_{11} = 1, 0^{\circ}$ $S_{12} = 0, 0^{\circ}$ $S_{21} \simeq 1.2, 180^{\circ}$ $S_{22} \simeq 0.9, 0^{\circ}$

Other geometry GaAs FETs have similar s-parameter values at the d.c. limit, the exact values of S_{21} and S_{22} depending on the device transconductance G_{mo} and drain resistance R_d respectively.

By extrapolating back from 1GHz and 2GHz s-parameter values reasonable agreement with the expected s-parameters at zero frequency is found. (See lines 6 and 7 of Table 6.1. and Fig.5.3.)This correlation between the simple d.c. FET model and measured parameters at low microwave frequencies, 1-2GHz, is reassuring and shows that no gross problems existed with the measurement system or procedures used. The theoretical prediction of device s-parameters at microwave frequencies, up to 12GHz, from the equivalent circuit is complex since all circuit elements must be considered including those associated with the device package.

With the use of a modified SLAP circuit analysis computer programme Slaymaker et al have shown good correlation between the measured s-parameters of LID packaged GAT 2 devices and equivalent circuit predictions up to 12GHz. The equivalent circuit was modified from that shown above to include package inductance and additional parasitic effects intrinsic to the FET chip.(23)

The general agreement between calculated and measured s-parameters from d.c. to microwave frequencies increasesconfidence in the validity of the characterisation technique. This was subsequently confirmed by comparison of calculated and actual amplifier circuit results.

CHAPTER VII.

Applications of GaAs Field Effect Transistors.

CHAPTER VII

APPLICATIONS OF GaAs FIELD EFFECT TRANSISTORS

The measured s-parameters of GaAs FETs reported in previous chapters predict that these devices should give useful amplifier gains at microwave frequencies. To confirm these predictions various amplifiers operating at different frequencies have been designed, built and assessed. Other potential applications such as oscillators and mixers have also been considered.

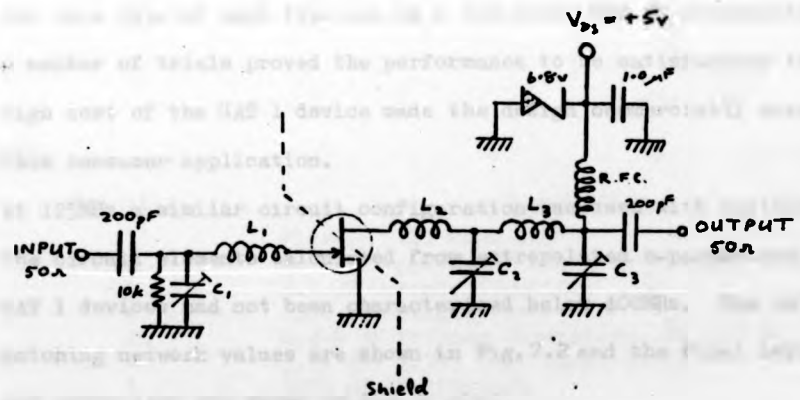
7.1. Low Frequency Amplifiers using Lumped Circuits

At frequencies up to about 2GHz amplifier circuits may be realised using conventional 'lumped' techniques where impedance matching is achieved by the use of suitable combinations of inductors and capacitors. The matching inductor and capacitor values may be determined using computer aided design (CAD) routines or for simple circuits by the use of Smith Chart techniques. To assess the performance of GAT 1 devices in such circuits two designs were developed and assessed at centre frequencies of about 125MHz and 800MHz respectively. These frequencies were chosen because of potential applications or amplifier interest in the respective bands. The 800MHz circuit was designed first and used a TO-72 packaged GAT 1 device in the grounded source configuration. The conjugate matching impedances S_{11}^* and S_{22}^* calculated from the measured s-parameters at 800MHz were used with a Smith Chart technique(24-26)to determine the matching circuit values, $L_1 - L_3$ and $C_1 - C_3$. Fig. 7.1

To simplify biassing requirements the FET was operated with zero gate bias, a d.c. return for the gate being provided by a 10 kilohm resistor in parallel with C_1. The drain bias was supplied via a RF choke, decoupled at the connector end by a 1μF capacitor with a 6.8V zener diode in parallel for over and reverse voltage protection. To prevent coupling between the input and output matching circuits and hence possible instability, a metal screen was used to isolate the gate and drain leads of the TO-72 package.

TABLE 7.1 800 MHz GAT 1 AMPLIFIER PERFORMANCE

Power gain	15 dB
Operating frequency	700MHz to 900MHz
Bandwidth (-1dB)	200MHz
Noise Figure	3 dB
Input and Output Return Loss	>5 dB
Reverse isolation	>30dB
Intermodulation 3rd order intercept point	+27dBm
Power requirements, d.c.	+5 Volts, 50mA maximum.



L_1 = 22 nH C_1 = 6 pF

L_2 = 45 nH C_2 = 4 pF

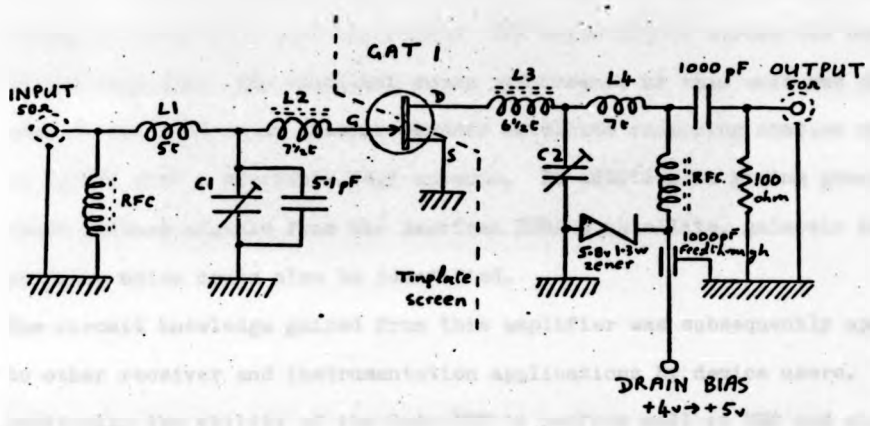
L_3 = 13 nH C_3 = 5 pF

Fig: 7.1. Circuit diagram

In the completed amplifier trimmer capacitors were used for $C_1 - C_3$ and adjusted to give the required gain and frequency response as indicated by the network analyser. The performance of the amplifier after alignment is shown in Table 7.1 and the circuit diagram in Fig. 7.1.
The gain and bandwidth achieved are as expected for a GAT 1/010 device however the noise figure at 3dB is not as low as could be achieved under optimum conditions. In this case the circuit was optimised for gain and frequency response with noise figure a secondary consideration. The difficulty in matching GaAs FETs at this frequency is shown by the low values of the input and output return losses obtained. The amplifier exhibited good linearity and using a two tone intermodulation test gave a third order intercept point of +27dBm.
This latter parameter was of particular interest for one potential application which was as a sustaining amplifier in a Surface Acoustic Wave (SAW) oscillator being developed by Plessey. Another possible application for this type of amplifier was as a low noise UHF TV preamplifier. While a number of trials proved the performance to be satisfactory the relative high cost of the GAT 1 device made the design commercially unviable for this consumer application.
At 125MHz a similar circuit configuration was used with initial values of the circuit elements calculated from extrepolated s-parameters since the GAT 1 devices had not been characterised below 400MHz. The calculated matching network values are shown in Fig. 7.2 and the final amplifier circuit and parts list are shown in Fig. 7.2(b).
To simplify the realisation of the larger inductances, L2 and L3, these were wound on formers with low loss ferrite cores. Since the device was only conditionally stable at these frequencies, it was not possible to conjugately match both the input and output. The 100 ohm resistor across the output enabled the device drain to be mismatched as an aid to stability and bandwidth yet keeping the amplifier output VSWR reasonable. The loss associated with this resistor reduced the gain slightly, but had little effect on the noise figure.

L1	=	.10μH	L3	=	.31μH
L2	=	.45μH	L4	=	.17μH
C1	=	9 pF	C2	=	7 pF

Fig. 7.2. Calculated matching network values for 125MHz amplifier.



COMPONENTS

Quantity	Description
1	Plessey GAT1 GaAs FET
2	RS 2A Suppressor Chokes or Similar 6–10 μH RF Chokes
1	5.1 pF Ceramic Capacitor
1	1000 pF Ceramic Capacitor
2	0.4–6 pF Trimmer Capacitors, C1 and C2
1	5.8V (or 6.2V) 1.3W Zener Diode
1	1000 pF Feedthrough
1	100 ohm Resistor

Miscellaneous: Diecast box 89 x 35 x 30 mm; connectors, tinplate for screen.

Fig. 7.2.(b) Final 125MHz amplifier circuit and parts list.

RF chokes were used to DC ground the FET gate and to apply the drain bias. The latter was again applied via a 1000pF feedthrough shunted with a 1μF decoupling capacitor and with a 5.8V 1.3W zener diode to prevent excessive or reverse biassing.

The amplifier was constructed in a small diecast box with a central tin-plate screen to isolate the input and output matching circuits. Fig. 7.3. After construction the circuit was aligned for the best gain response over the 100–150MHz frequency band by adjusting the trimmer capacitors C_1 and C_2. The completed amplifier had a peak gain of 25dB at 120MHz and from 105MHz to 151MHz the gain was $>$ 23dB. The noise figure across the band was better than 1dB. The excellent noise performance of this unit was confirmed when it was used in an amateur weather satellite receiving station operating at 137MHz with a steerable Yagi antenna. In addition to giving good cloud cover picture signals from the American ESSA 8 satellite, galactic sources of radio noise could also be identified.

The circuit knowledge gained from this amplifier was subsequently applied to other receiver and instrumentation applications by device users. In particular the ability of the GaAs FET to perform well at VHF and at reduced temperatures lead to its use in nuclear magnetic resonance (NMR) cyrogenic systems. At liquid nitrogen temperatures 77° K noise figures of less than 0.3dB have been obtained from GAT 1 devices at 129MHz.(27)

7.2. Microstrip Circuit Microwave Amplifiers

For frequencies above 2GHz 'lumped' circuits of the type discussed above become impracticable and 'distributed' circuits consisting of transmission lines of varying impedance and lengths are used instead. With the correct choice of transmission line elements the FET impedances may be matched as required, for noise figure or gain performance to realise amplifier modules. While in theory various kinds of transmission line could be used such as co-axial or stripline in general the most common is microstrip.(28)

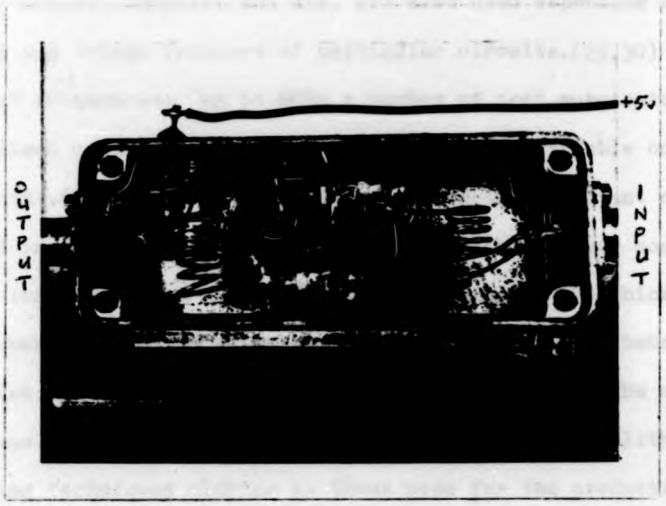


Fig. 7.3. Internal view of 125MHz amplifier showing construction.

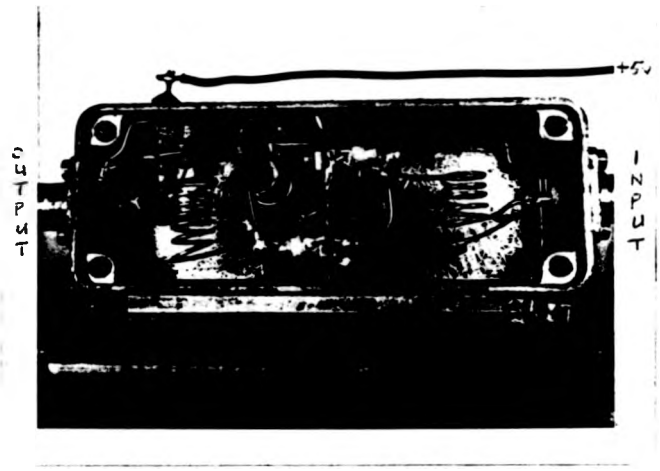


Fig. 7.3. Internal view of 125MHz amplifier showing construction.

Microstrip transmission lines consist of a conductive track supported over a single ground plane. The area between the track and groundplane is filled with a dielectric substrate often alumina or a 'plastic' material onto which the metal conductive surfaces have been deposited. Other dielectrics including quartz, sapphire and air, are also used depending on the operating frequency and design features of particular circuits.(29,30)

For use at frequencies up to 8GHz a number of test substrates and amplifiers were realised using a 'plastic' type of material available commercially as Polyguide.(14) This material with a dielectric constant of 2.32 was purchased in sheets 0.023 inch thick having a thin copper coating one side and a 0.25 inch aluminium ground plane on the other. The thick ground plane enabled connectors to be attached directly to edges of substrates and facilitated the mounting of FETs and other components. The microstrip circuit was defined on the copper coated face using photolithographic and etching techniques similar to those used for the production of printed circuit boards. The relative low cost and ease of processing of 'plastic' substrate material makes it ideal for development work with packaged devices. It is not however suitable for use with chip devices since it is not compatible with the bonding process. Where chip devices have been used gold plated alumina ceramic substrates were used for microstrip circuits. Test amplifiers on Polyguide were designed and constructed for operation at 1.5GHz and 3GHz centre frequencies using GAT 1 and GAT 2 devices respectively. Both circuits were originally based on LID packaged device s-parameters, but later modified to accept P103 packages.

A comparison of the measured and calculated performance of the 3GHz circuit Fig.7.4 with P103 devices was carried out. The performance of the circuit shown in element form in Fig.7.5 was analysed using a CAD routine called DEMON, implemented on the Sigma V computer, with computer corrected s-parameter data for a GAT 2/P103 device. (31) Table 7.2.

The application of the Sigma V to computer aided design formed part of a separate research programme which contributed to the understanding and application of GaAs FETs in microwave amplifiers. (32)

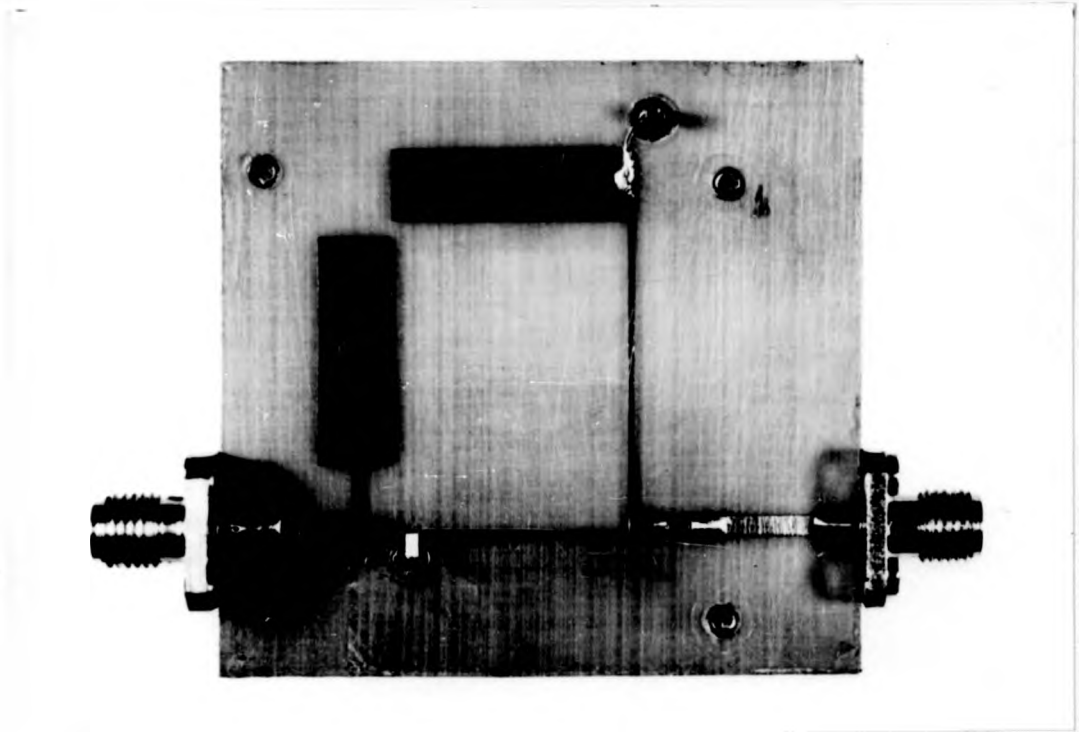


Fig. 7.4. 3GHz amplifier on Polyguide.

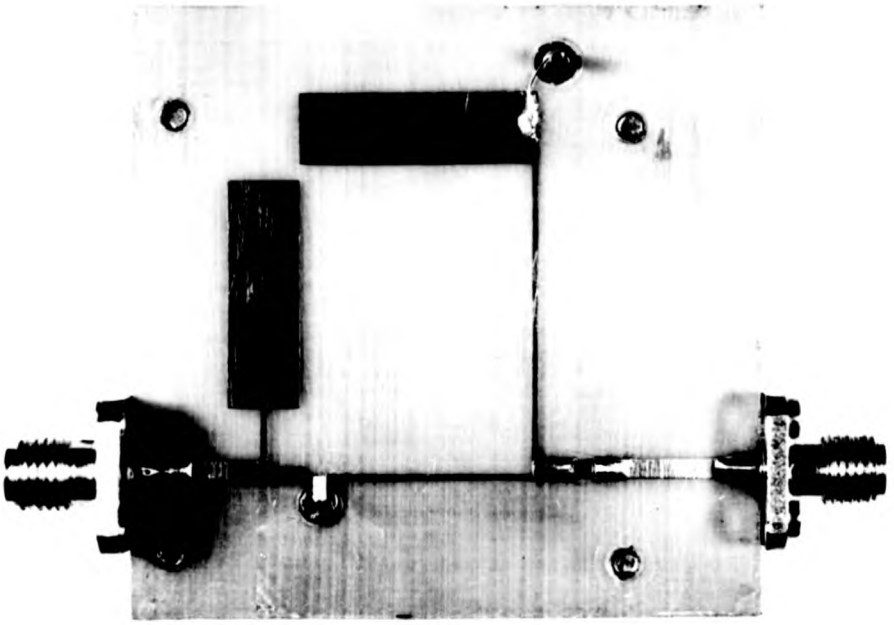


Fig. 7.4. 3GHz amplifier on Polyguide.

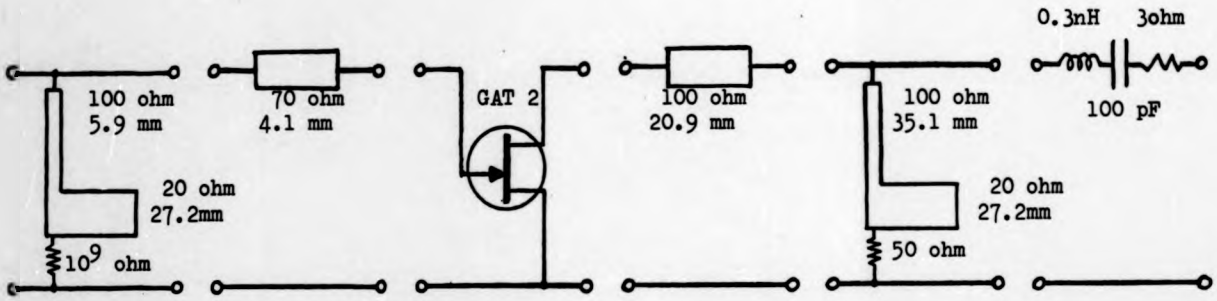


Fig: 7.5. Circuit elements used to realise a single stage S-band FET amplifier

Table 7.2. S-parameters of GAT 2/P103 device used in single stage S-band amplifier circuit.

Frequency GHz	S_{11} Mag.	S_{11} Ang.	S_{12} Mag.	S_{12} Ang.	S_{21} Mag.	S_{21} Ang.	S_{22} Mag.	S_{22} Ang.
2.0	.83	- 57	.047	68	1.79	127	.84	-22
2.5	.73	- 72	.059	62	1.74	118	.82	-27
3.0	.67	- 85	.066	61	1.64	104	.83	-32
3.5	.63	- 95	.062	69	1.5	97	.80	-33
4.0	.54	-110	.061	77	1.46	89	.79	-37

The same device whose s-parameters had been used in the circuit analysis was installed in the actual circuit and the resulting amplifier gain and VSWRs measured. The calculated and measured results for the gain, input and output reflection coefficients are shown, Figs.7.6to 7.8, While the shapes of the calculated and measured responses are similar the latter are offset at a lower frequency about 150MHz removed from the calculated results. This apparent discrepancy is however consistent with a known error in the device s-parameters. The error was due to the neglection of the through length of the calibration line since the option to allow for this had not been incorporated into the correction programme at the time of the device measurements. As a result the phase angles of S_{12} and S_{21} are in error at 3GHz by about 10^{o}, the electrical length of the 2mm through connection. The effect on the main parameter S_{21} is equivalent to frequency offset downwards of several hundred MHz which is reflected in the measured amplifier response. These calculations and measurements were useful in confirming:

a) CAD routines are applicable to FET amplifier analysis.
b) Reasonable agreement can be obtained between theory and practice.
c) Accurate device s-parameter data is crutial in achieving satisfactory circuit designs.

At frequencies above 8GHz difficulties of determining exact s-parameters for chip devices (section 6.4) and precisely realising circuit elements lead to the exploration of alternative ways of producing FET amplifiers.

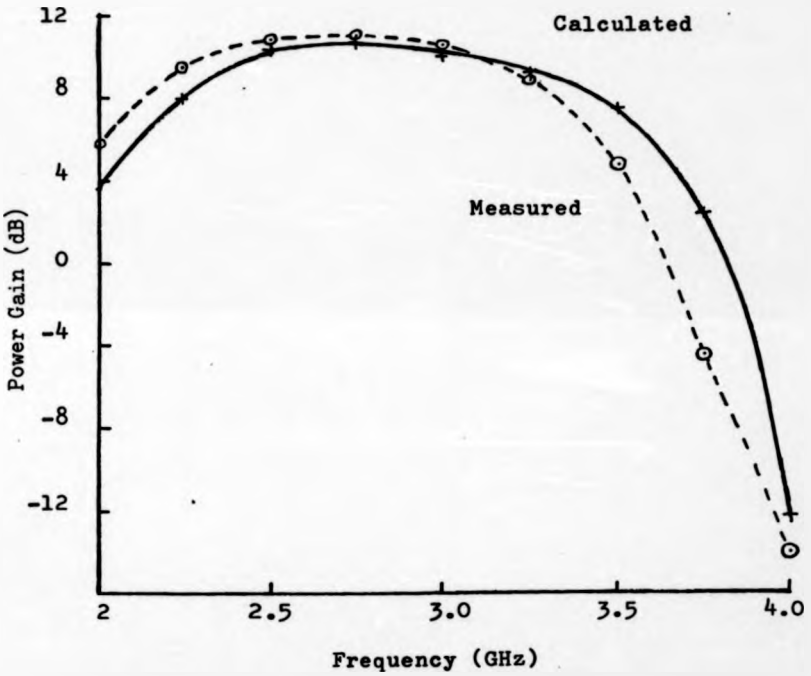


Fig: 7.6. Measured and calculated gain response of single stage S-Band F.E.T. Amplifier

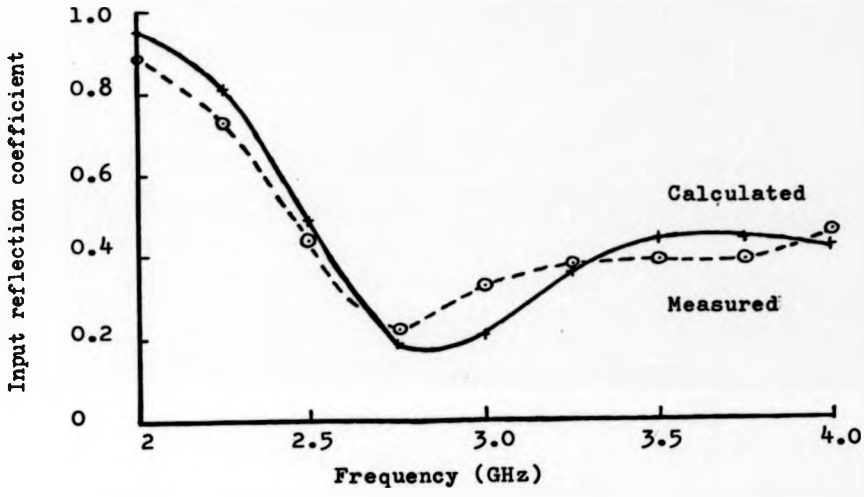


Fig: 7.7 Input Reflection Characteristics of S-Band Amplifier

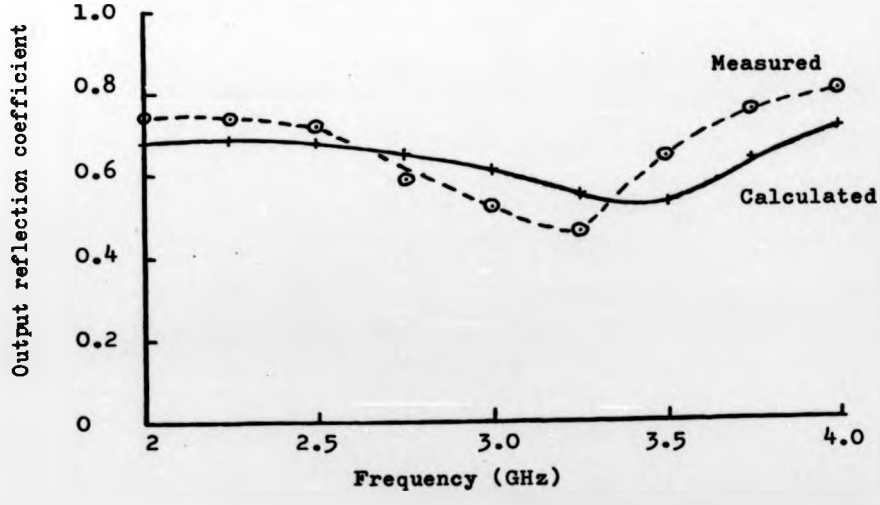


Fig: 7.8 Output Reflection Characteristics of S-Band Amplifier

7.3. Tuned Amplifiers with Chip FETs

A tuning technique on microstrip was developed to overcome the above problems and allow the amplifier performance of GaAs FETs at X-band frequencies to be explored. This was first used to enable the amplifier performance of chip devices on alumina test substrates to be compared with S-parameter gain predictions. Single stage amplifiers were produced by placing metal discs, 3mm in diameter on the 50 ohm input and output lines of the substrate and positioning them to obtain the best input and output matching and hence maximum gain. The discs effectively act as shunt capacitors, whose value may be changed by varying the diameter and by positioning this 'capacitor' an appropriate distance from the device the equivalent LC network produced matches the device impedance to the 50 ohm test system. At 11GHz with one disc on the input line and two on the output line single stage amplifier modules with gains of 6-7dB were realised. Fig. 7.9 The equivalent circuit of these modules can be represented as inductors (lengths of 50 ohm line) and shunt capacitors (discs) as drawn in Fig.7.10. Not unexpectedly there is a striking similarity between this and the circuits described previously for lower frequency amplifiers.

The tuning technique was applied to three stage circuits to obtain higher amplifier gains and confirm that GaAs FETs could be cascaded in such circuits. In these amplifiers three GAT 3 device chips were mounted on an alumina substrate 2 x 1 x 0.025 inches on which bias filters and 50 ohm interconnecting lines had been defined by normal photolithographic and etching MIC techniques. At the ends of the 50 ohm lines adjacent to the devices GaAs MOS type chip capacitors were used to isolate the d.c. bias which was applied via bond wires from the bias network.

With the alumina circuit mounted in its box and connected to the network analyser, metal tuning discs were positioned on the 50 ohm transmission lines to obtain the required gain frequency response. When the desired performance had been achieved the discs were permanently fixed to the substrate. Fig.7.11 shows the method of construction of the amplifier.

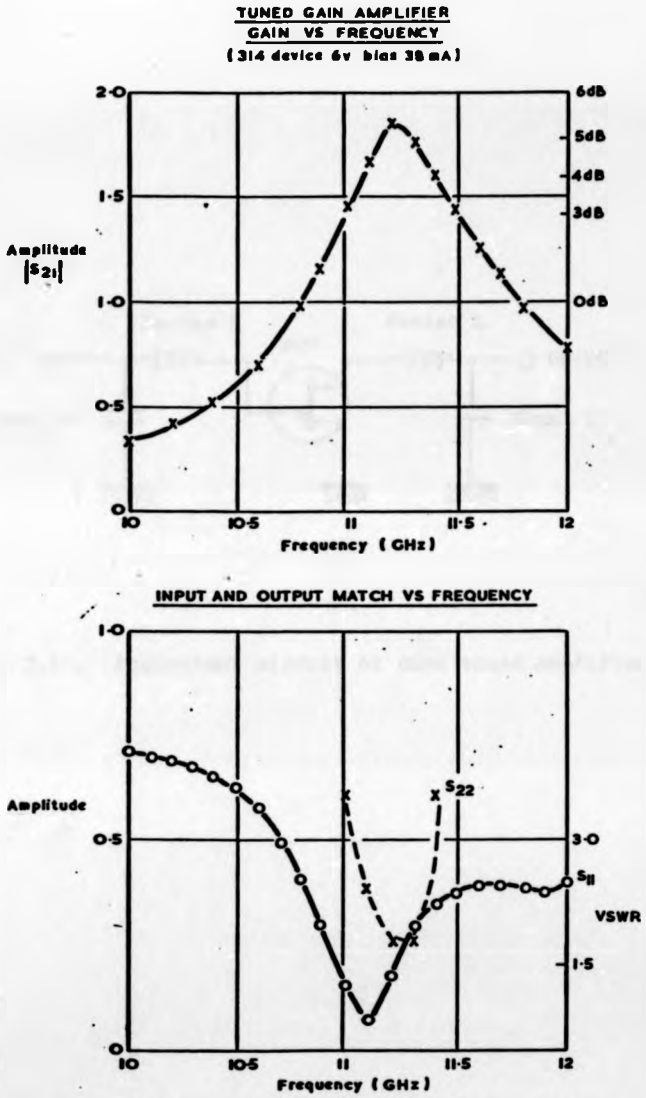


Fig. 7.9. Performance of single stage disc tuned amplifier.

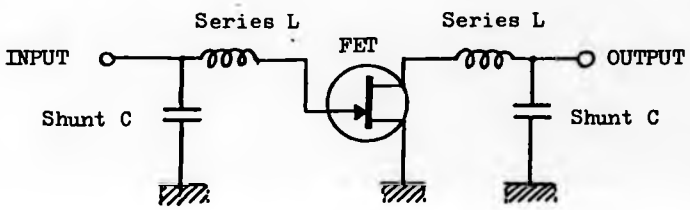


Fig: 7.10. Equivalent circuit of disc tuned amplifier.

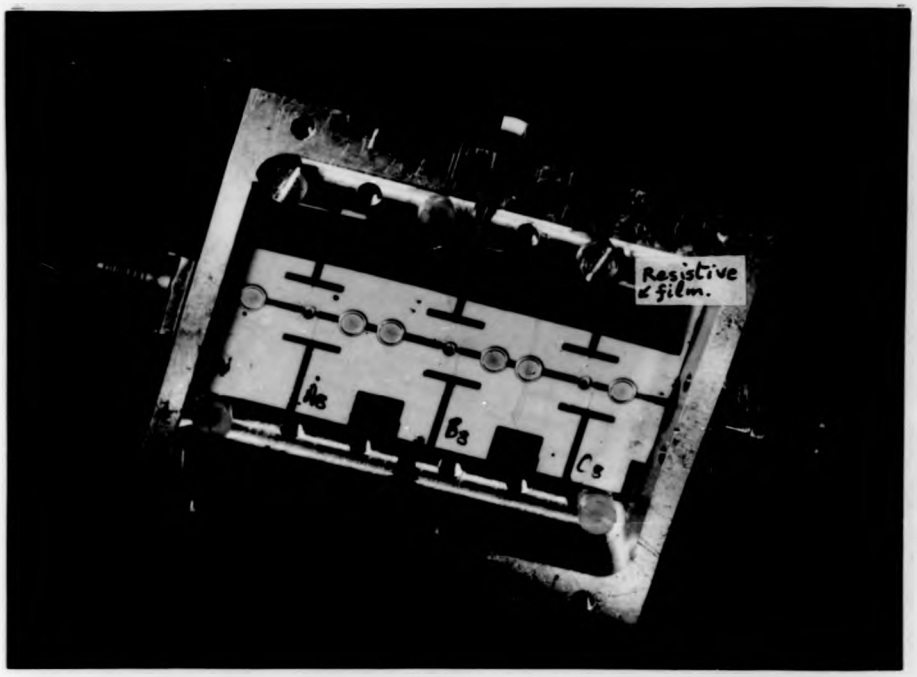


Fig. 7.11 X-band amplifier construction.

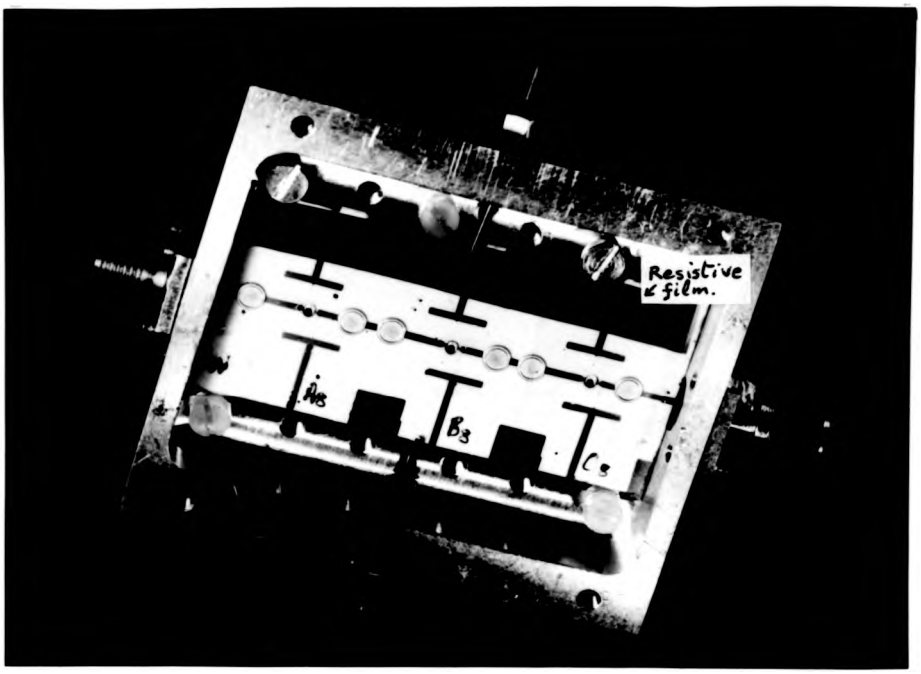


Fig. 7.11 X-band amplifier construction.

The resistive film attached to the gate bias networks introduces loss at out of band frequencies hence stabilising the devices and preventing low frequency oscillations.

The tuning technique proved versatile and is ideally suited to producing prototype amplifiers and for evaluating devices. It is quick, inexpensive and tolerant of device parameter variations, yet capable of realising the full potential of the FETs being used. (33)

To determine the feasibility of realising high (> 40dB) gain FET amplifiers at X-band for potential microwave I.F. applications a number of three stage disc tuned modules were produced. One such unit consisting of two modules cascaded with isolators for good VSWRs and having 42dB gain at 11.2GHz is shown. Fig. 7.12.

In addition to the frequency response, measurements were also made to determine other parameters such as gain variation with temperature, intermodulation and output power characteristics. These results are shown in Table. 7.3.

A second amplifier of similar performance was also produced, but this incorporated a thermistor, temperature sensing circuit to control the negative gate bias applied to the first module. This compensation circuit reduced the gain variation with temperature to less than 1dB total with the minimum gain occuring at 20°C.

Results obtained from the above amplifiers confirmed the viability of producing high gain GaAs FET amplifiers suitable for satellite and other system applications. The disc tuning technique was subsequently used at other frequencies for performance assessment and is still used on many sophisticated MICs as a means of 'fine tuning' to overcome effects of slight variations in device or circuit parameters.

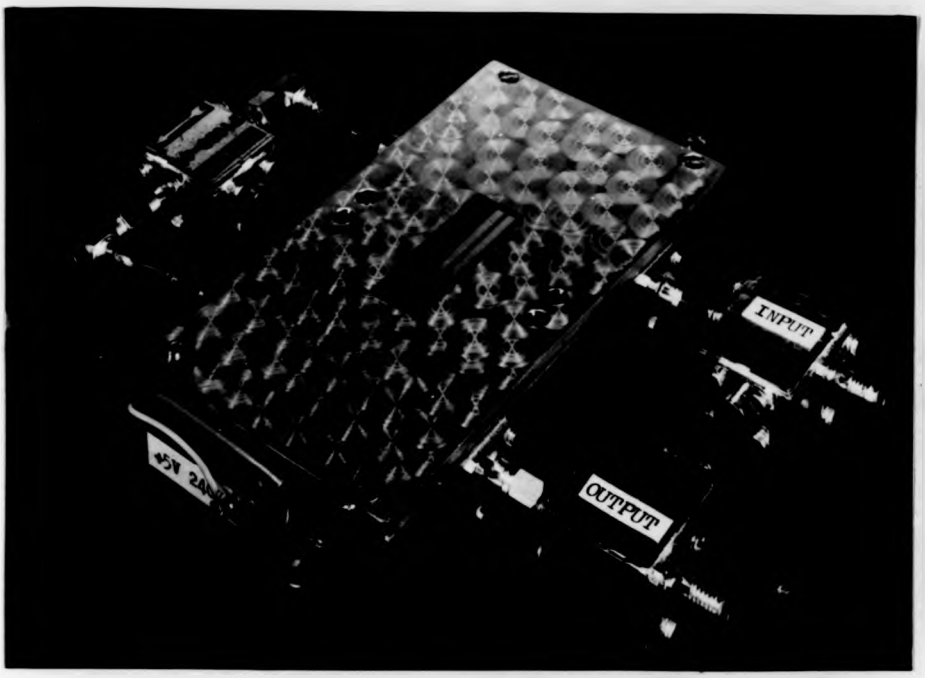
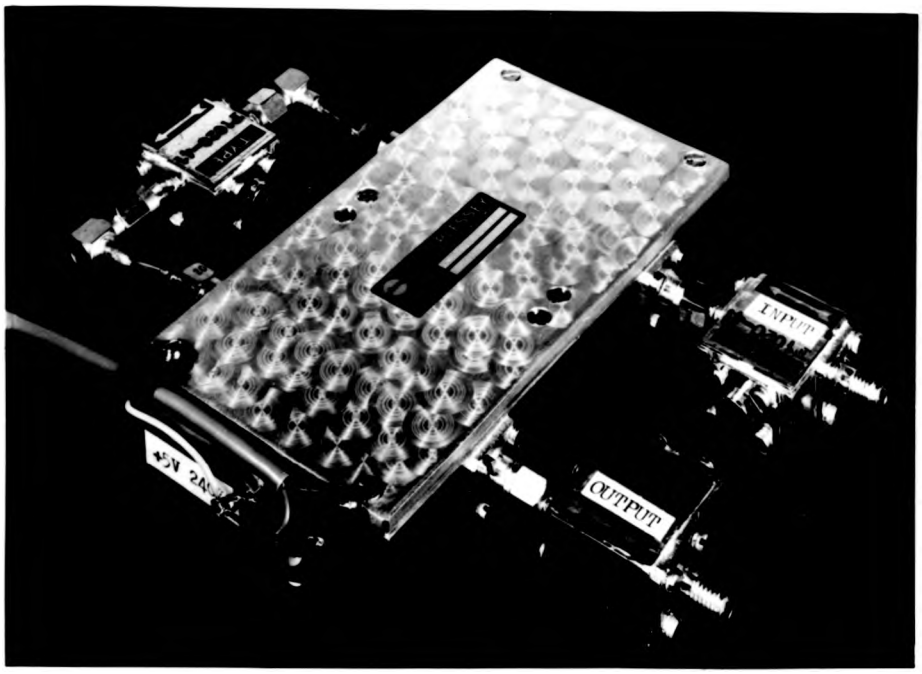


Fig. 7.12. 42dB gain 11.2GHz amplifier.

Table 7.3. 11.2 GHz AMPLIFIER PERFORMANCE

Centre frequenoy	11.18 GHz
Bandwidth at -1 dB points	260 MHz
Gain (at 20°C)	42 dB
Noise figure (at 20°C)	13.5 dB
Input and Output VSWR's	1.5
Gain variation 7°C - 35°C	± 1.2 dB
Third order intermodulation level at output for two equal carriers at input of -50 dBm each	- 40 dB
Output power level	8.5dBm



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Output power level	8.5dBm

7.4. Low Power Consumption Amplifier Operation

One critism of early FET amplifiers such as the 11.2GHz unit described above concerned their relatively high d.c. power consumption compared with low noise tunnel diode amplifiers. This high power consumption resulted from the drain current of each FET typically being a few tens of milliamps. For example the 42dB gain 11.2GHz amplifier module required 1.2W and at lower frequencies a typical 2-stage C-band amplifier giving 15dB gain needed 0.3W of bias power.

The reduction of FET amplifier power requirements was investigated and by using suitable devices appropriately biassed the dc, power consumption has been reduced by an order of magnitude. Results were obtained for a two-stage amplifier with a centre frequency of 7.4GHz which illustrate that low power consumption GaAs FET amplifiers for applications such as satellite communication systems with only limited power supplies could be readily produced.

For low power operation devices which exhibit drain current saturation at low drain source bias voltages and good transconductance values at drain currents of a few milliamps are required. GAT 3 devices in P103 packages from a batch having drain current saturation voltages of 1.5V to 2V and gate pinch off voltages of -1.5V to -2V were selected which satisfied these requirements. Fig.7.13 The transconductance of these devices falls slowly with decreasing drain currents from 10 mmhos at 12mA to 4 mmhos at 1mA.

The GaAs FETs were mounted in a two stage narrow band amplifier designed for C-band operation. This amplifier fabricated on Polyguide dielectric material utilised low impedance sections of microstrip line to match the input and output of the FET to 50 ohms at the frequency of interest. The design was optimised for maximum gain using the device parameters measured at bias values of V_{DS} = +5V and V_{GS} = 0V. The gain response of the amplifier was measured using the network analyser under various device bias conditions. Reducing the drain bias voltage V_{DS} from +5V to +2.5V with zero gate bias gave little change in the gain response. Below about +2V the response became distorted due to a fall off in gain at the higher frequencies. The drain bias voltage

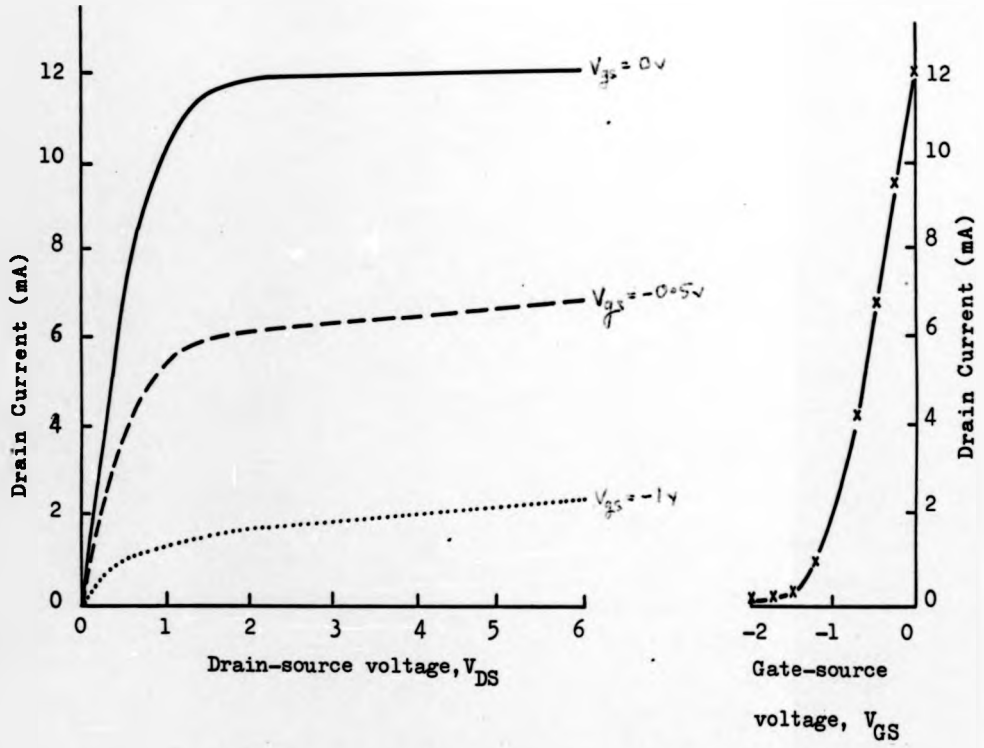

Fig: 7.13. D.C. characteristics of GaAs FETs, suitable for low power operation.

was fixed at +2.5V, this being the lowest value commensurate with maximum gain and bandwidth.

By applying the same negative gate bias to both devices, the total drain current was reduced and the gain response remeasured.Fig.7.14 The reduction in current leads to a fall in the amplifier gain, but has little effect on the shape of the gain response until the current through each device drops below about 2mA. Even at 2.5mA total current however 9dB of gain was available for an input d.c. power of only 6.25mW.

The fall in gain, with V_{DS} fixed and decreasing drain current, due to negative gate bias is shown.Fig.7.15.Also shown is a plot of the gain for each 10mW of d.c. power against the total drain current. As the current is reduced the gain decreases, but at a slower rate than the d.c. supply power. The gain for each 10mW of d.c. power therefore increases and reaches a peak of 14.5dB/10mW at about 2.3mA drain current. At lower currents the gain falls off very rapidly as both FETs pinch off.

For the two stage amplifier investigated the optimum low d.c. power performance occured with a supply current of about 5mA. It then gave 13dB of gain at 7.4GHz with a -1dB bandwidth of 200MHz. The measured noise figure under these conditions was less than 7dB although no attempt had been made to minimise it. Intermodulation measurements indicated there was little degradation in the performance at low bias levels. A dip of almost 10dB in the magnitude of the third order I.M. products was observed for intermediate drain currents of 4mA to 6mA per device due to the nearer square law characteristics of the FET at these values. Under low bias conditions, with two signals each giving -10dBm at the amplifier output, the third order I.M. products were 30dB down on the fundamental. This corresponded to an Intercept Point of +5dBm.

This study showed that GaAs FETs could compete with other devices in limited supply power situations and still retain the established GaAs FET advantages of stability, reliability and linearity compared with tunnel diode amplifiers.

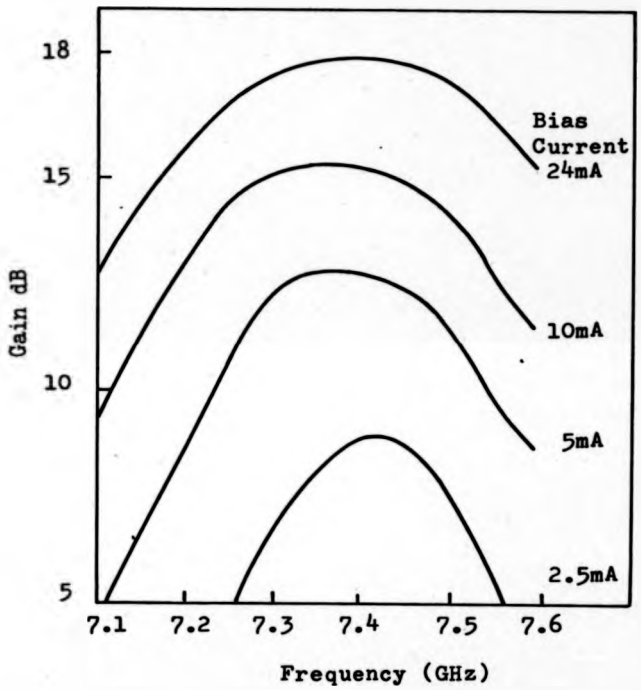

Fig: 7.14. Gain response versus bias current for 2-stage C-Band FET amplifier, with V_{DS} = 2.5 volts.

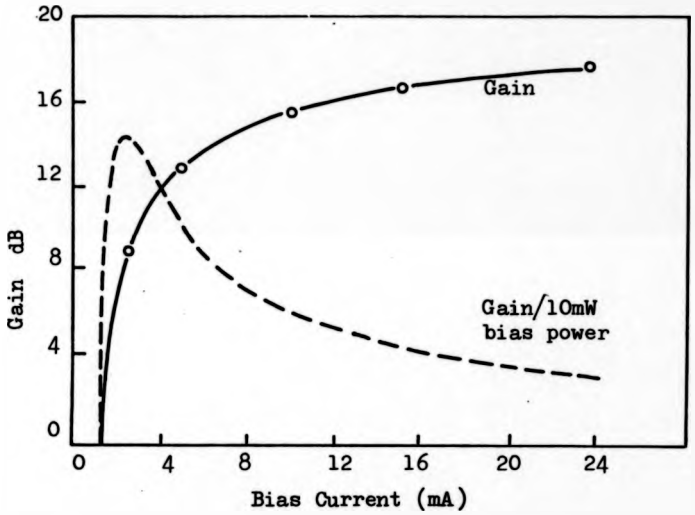

Fig. 7.15 Gain characteristics versus bias current and power for 2-stage C-Band FET amplifier.

7.5. GaAs FET Oscillators

A number of different types of oscillator circuits were studied at frequencies from L to J-Band to assess the performance of FETs in this application.

At frequencies up to S-band versions of the Hartley oscillator configuration were used.(34). Above 1GHz microstrip circuits were produced using a short circuit stub slightly less than $\lambda/4$ long which was resonated with the gate capacitance of the FET. The device source connected to a tapping point on the stub and the RF output was taken from the drain via a 50 ohm transmission line which also contained the d.c. bias feed. The approximate stub length required to resonate with the gate capacitance at a given frequency was determined from a Smith Chart plot of the device input s-parameters. For a GAT 3 device at 3GHz it is found that a stub of length 0.21λ or electrical length 21mm is needed to resonate with the S_{11}. Such a circuit fabricated on polyguide dielectric material is shown. Fig.7.16. This circuit incorporates a 1000pF chip capacitor in the resonant stub, a later modification to allow self biasing of the device gate. The actual resonator stub length realised on the final circuit was 21.6mm and with a GAT 3 device (Batch 388B) the measured oscillation frequency was 3.02GHz. The original circuit gave output powers $>$ 20mW with efficiencies of 10%.Fig.717.When modified to self biasing of the gate similar output powers were obtained, but with increased efficiency of 38%. The output power in both cases increased linearly with d.c. bias up to the maximum value applied of V_{DS} = +7V. Maximum oscillator efficiency occured at +5 to +6 volts drain bias. At frequencies above S-band the Hartley oscillator circuit becomes impracticable and the Colpitt configuration, which makes use of the internal feedback of the device, is more suitable. Experimental X-band circuits fabricated on polyguide using LID packaged FETs yielded output powers of 5 to 10mW with efficiencies of 10 percent.

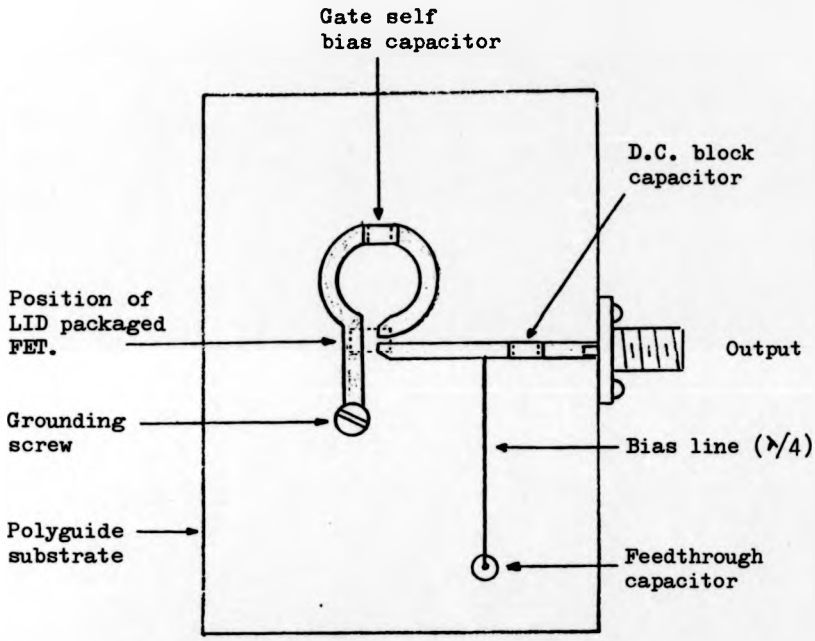

Fig: 7.16. FET oscillator circuit on

Polyguide, operating frequency 3GHz.

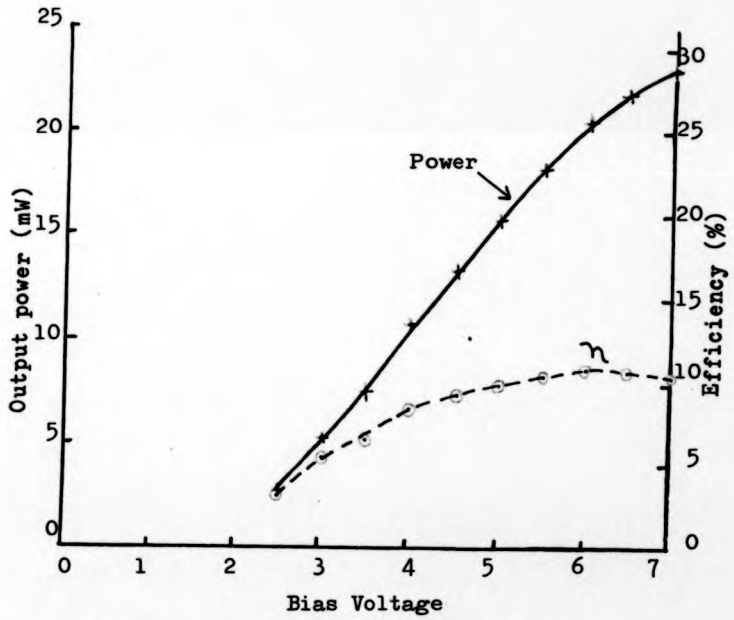

Fig: 7.17. Output power and efficiency of initial 3GHz oscillator circuit.

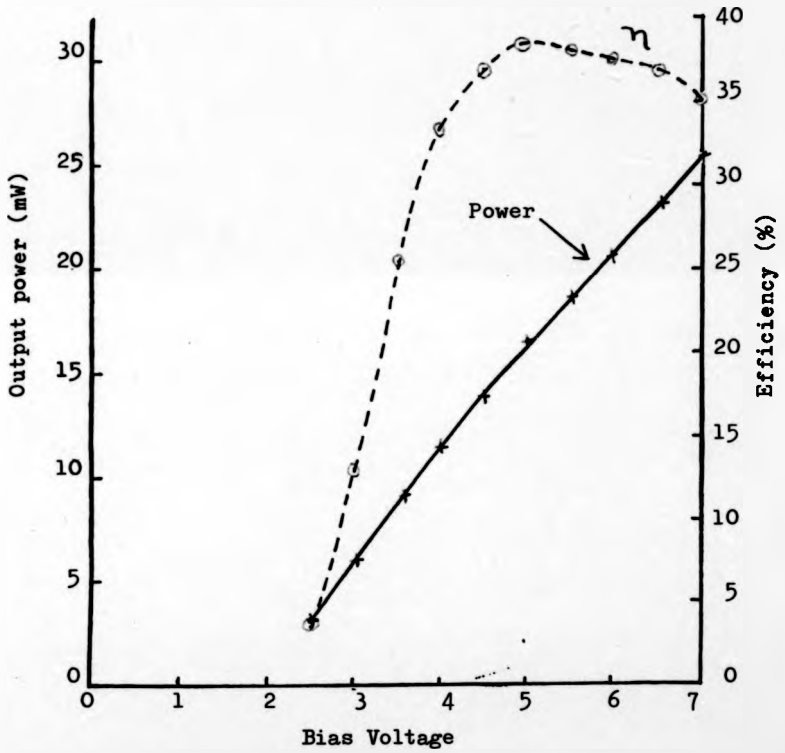

Fig: 7.18. Output power and efficiency of 3GHz oscillator with gate self bias circuit

At J-band device chips mounted directly onto alumina substrates have been used with chip capacitors and bond wires forming the resonant circuit. Microstrip output lines and bias networks were defined on the substrate using normal MIC techniques.

Prototype oscillators using GAT 3 device chips in such circuits oscillated at 13 to 15GHz. Results for a 13GHz oscillator are shown. Fig.7.19,The maximum output power was 14mW at +6 volts drain bias with an efficiency of 9 percent. At higher drain bias levels the output power and efficiency both decrease, probably due to the poor heat sinking of the active device.

Pulling range measurements, not unexpectedly, gave a low Q of about 50 for this circuit which was also reflected in the rather broad spectrum of the RF output. This could be improved by the use of higher Q circuits or by coupling to other resonant structures. (35,36)

This investigation has shown that GaAs FETs are useable as oscillators up to J-band frequencies with output powers of a few tens of milliwatts. The striking feature of the FET oscillator, even in the experimental circuits described, is its efficiency which is higher than other solid state sources such as Gunn devices.

7.6. Other Applications

While the prime use of GaAs FETs is in microwave frequency amplifiers it is also finding applications in other circuit functions. The FET oscillator was discussed in the previous section and other workers have shown the FET to be equally suitable as a mixer. The most significant characteristic of the mixer circuit is the greater dynamic range, approximately 10dB improvement, compared to conventional diode mixers. (37,38)

In addition to analogue applications, FETs of the Plessey GAT 2 type have been utilised as switches in experimental digital systems.(39) Existing n-channel depletion mode devices do however suffer a disadvantage in this role due to their relatively high drain currents and hence power dissipation.

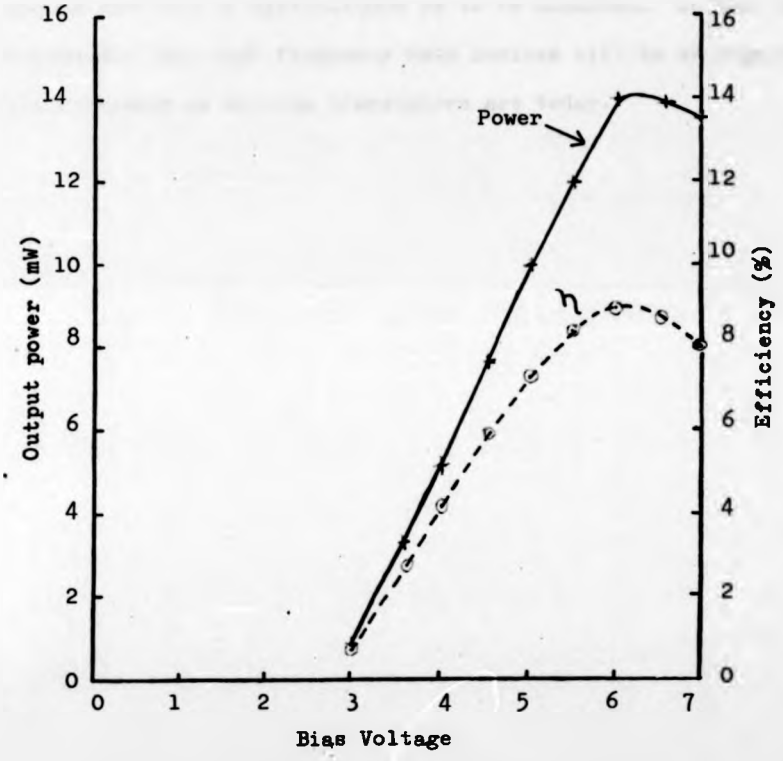

Fig: 7.19. Output power and efficiency of 13GHz oscillator using a GAT3 chip FET.

The high input impedance and low gate capacitance of GaAs FETs have been utilised in applications such as buffer amplifiers for RF sampling probes and in transconductance amplifiers for use with photodetectors.

As GaAs and FET technology matures the use of such devices in an increasing spectrum of applications is to be expected. In the longterm it is possible that high frequency GaAs devices will be as significant in future systems as silicon transistors are today.

CHAPTER VIII.

Conclusions and recommendations.

CHAPTER VIII

CONCLUSIONS AND RECOMMENDATIONS

8.1. General

An automated and computer corrected s-parameter measurement system has been realised by interfacing a manual Hewlett Packard type 8410 network analyser with the Sigma V computer in the Engineering Department at Warwick University.

This measurement system was used, with various calibration routines, to assess GaAs FETs of differing designs and fabrication techniques mounted in a range of package configurations. Subroutines in the measurement computer programme enabled gain performance of devices to be calculated from the corrected s-parameters hence facilitating the comparison of devices.

Effects on RF performance of design or process changes were communicated to the device manufacturer in order to assist with its development. Use was also made of the s-parameter and gain data obtained on various devices to assess their usefulness in certain applications and to realise test circuits for demonstrating potential performance. A number of amplifiers and oscillators incorporating these GaAs FETs were constructed and characterised at operating frequencies in the range 0.1 to 12GHz. Although experimental, the results from these circuits illustrated that GaAs FETs are capable of excellent performance over a wide frequency range.

8.2. Computer corrected s-parameter measurement system

In developing the hardware and software for this system particular emphasis was placed on its suitability for characterising active microwave devices and in particular FETs. As a result some compromises were made which could lead to difficulties in other applications.

The use of the Hewlett Packard s-parameter test set with the 2-port correction programme has the advantage that all measurements on the device under test can be carried out in one operation without the need to manually reverse the device as is the case with the single port programme. The penalty for this convenience however is a slightly degraded accuracy arising from imperfections in the s-parameter test set. For FET measurements however, the accuracy of typically better than $\pm$ 0.02 in amplitude and $\pm$ 2.5^{o} in phase is acceptable and is considerably better than can be achieved by purely manual systems.

Where the highest measurement accuracy is required the use of the single port correction programme together with the reflectometer test box is recommended.

A number of residual sources of error still exist in the measurement system, the most significant of which is due to inaccuracies in the setting of the frequency of the microwave source. While periodic revision of the stored voltage versus frequency tables in the computer programme can take account of ageing effects the relatively poor frequency stability of the sweep oscillator may result in deviations of several MHz from the desired frequency. The resulting errors in corrected s-parameter measurements increases as the electrical length between the network analyser Reference and Test channels becomes larger. When characterising FETs the system was first manually adjusted to approximately equalise the Reference and Test channel path lengths to minimise this source of error.

Two possible solutions to this problem were investigated, but not included in the system due to lack of time. One involved using the frequency counter to read the frequency at each measurement point and if this deviated from the required value a correction signal could be generated.

The second method which offered much improved frequency accuracy and stability was based on phase locking the sweep generator to the harmonics of a crystal oscillator using a Microwave Systems Inc., Microwave oscillator frequency stabiliser. (40). Where highest accuracy measurements are needed the implementation of the latter approach should prove worthwhile. Imperfections and nonlinearity effects in the network analyser and sampling head are other potential sources of error, but these are negligible when making transistor measurements.

Care must be taken when measuring high gain devices such as multistage amplifiers to avoid dynamic range limitations of the network analyser. At frequencies above 13GHz the performance of the system degrades, but this is to be expected since the s-parameter test set and parts of the network analyser are only designed for operation to 12.4GHz.
For the application considered, the characterisation of GaAs FETs, the consistent performance and special features of the system developed at Warwick have proved invaluable and yielded a wealth of s-parameter data (see Appendix).

8.3. Device Characterisation

The requirements for test fixtures and calibration standards for various packages have been considered and successful hardware designs and calibration procedures developed for handling LID and P103 packages. Attempts to characterise chip devices were not so successful because of problems with test mounts and calibration pieces. As a result of these difficulties and the destructive nature of testing chip devices this was abandoned early in the investigation.
Measurements of LID packaged FETs have established s-parameter and gain performance values for different devices under various test conditions.

These results have helped the development of the FET device by identifying such things as the superior performance of aluminium versus nickel as a Schottky gate metalisation and the poor gate to bonding pad contact on early electron beam defined devices. As important, but less spectacular, has been the ability to identify small performance differences resulting from processing or material property changes, so that the value of such changes could be accurately assessed.

Results obtained with devices in the P103 package confirmed that it was more suitable as a high frequency package than the earlier LID package design. The P103 package was used to assess initial samples of a wide gate geometry FET which subsequently became the Plessey GAT4 commercial device. To obtain information for performance assessment and circuit design other types of FET were also measured in P103 packages. Since this investigation was completed the LID package has been discontinued in favour of the P103 which offers better performance and ease of handling. A range of other packages designed for use with microwave FETs are now becoming available, a study of which could form a useful extension of this investigation.

8.4. GaAs FET Applications

Small signal amplifiers with operating frequencies in the range 0.1 to 12GHz have been realised with GaAs FETs[41] Most notable are a high gain 40dB unit at 11.2GHz and a low noise, low frequency, 125MHz design. At intermediate frequencies a comparison of the measured and calculated performance of an amplifier circuit with specifically characterised devices has shown that computer aided design (CAD) can be usefully applied to FET circuits. When fabricating the amplifier circuits lumped or distributed circuit techniques were used as appropriate to the operating frequency.

The amplifiers produced were characterised in terms of their gain response, noise figure and intermodulation performance. These results have shown that across the frequency range investigated the GaAs FET is capable of satisfying small signal low noise amplifier requirements. Even at frequencies below about 6GHz, where the FET has to compete with bipolar transistors, the lower noise figure and better intermodulation performance of the FET will ensure its future use.

Experiments with FET amplifier stages operated at low drain voltages and currents have shown that where necessary the d.c. power consumption can be reduced to levels compatible with other devices such as tunnel diode amplifiers.

Oscillator circuits incorporating FETs have yielded output powers of a few tens of milliwatts with good efficiencies. At 10GHz the FET oscillator is more than twice as efficient as a Gunn oscillator of similar power. The FET unit also operates at lower supply voltages which is advantageous in some applications. One disadvantage of the experimental FET circuits however, was their relatively poor frequency stability and noise performance. This may have been the result of using unoptimised circuits and further study of these effects is merited.

Since the GaAs FET extends transistor performance well into the microwave region of the spectrum it is not surprising to find transistor circuits being increased in frequency by the use of this device. To this end other workers are studying such diverse applications as high speed switching and optoelectronic uses of GaAs FETs.(42)

Without question GaAs FETs and circuits using these devices will increase in importance in microwave and other future systems, possibly to such an extent that Gallium Arsenide will rival silicon as the major semiconductor material.

8.5. Comments

Since the completion of this investigation in late 1974 many advances have been made in the three areas of measurement techniques device technology and applications. Indeed it was the authors continued involvement in this blossoming field of research and development which led to a years' secondment to Plessey's Californian activity and contributed to the delay in the completion of this thesis! Throughout the thesis all results, conclusions and references relate to the situation at the time of the programme completion. While some of the findings may at this time be of less relevance many of the techniques developed and conclusions reached are still valid. Some of the more recent developments are summarised in the following paragraphs and while in some areas such as device technology, vast improvements in performance have been made in others, such as measurement hardware, little has changed over the last five years.

At the time the two port full correction network analyser system was developed by the author at Warwick no similar system was available commercially. The Hewlett Packard Model 8542 Automatic Network Analyser (ANA) system available at that time for about £200K offered corrected measurements, but due to limitations in memory size of the integral minicomputer only used a six element-error model which necessitated the reversal of the test device. The Sigma V computer used on-line at Warwick however, afforded sufficient memory to support the full twelve element 2-port error model. The Model 8542 ANA is now obsolete and its place taken by a system with solid state sources replacing the original backward wave oscillators (BWOs) and a desktop computer in place of the minicomputer. The heart of the microwave system is still the Model 8410 network analyser unit.

As Fitzpatrick (43) noted the major area of change has been that of the computer which has benefited from the 'explosion' in digital technology. Commercial ANA systems, model 8409B now available from Hewlett Packard use a desktop computer with 187 kilobytes of Read/Write memory which is more than six times the capacity of the original minicomputer. With these systems there is virtually no limit on the programme size and the full 2-port correction routine can be handled with ease. Although much more powerful the cost of the current system is about one third that of the original model 8542 ANA. While the basic error model for the correction procedure has remained the same the derivation of the calibration equations and their exact solution has been considered by various workers(44,45). Latest ANA systems use the explicit equations in place of the iterative method to solve for the corrected s-parameters originally employed.

The main problem with the presently available ANAs, which generally operate up to 18GHz, is rapidly becoming one of limited measurement range. Already experimental FETs and amplifiers are being produced with operating frequencies in excess of 20GHz work which is to some extent being hampered by the lack of suitable measurement equipment.

Dramatic developments in device technology over the past five years have resulted in the establishment of whole new families of solid state microwave devices as well as improvements in the original small signal low noise type of GaAs FET. Key developments over this time have been in the areas of power FETs, monolithic microwave circuits on GaAs and GaAs integrated circuits. (46,47)

Power GaAs FETs are now commercially available with output powers of about 1 Watt at frequencies in excess of 12GHz. At lower frequencies power outputs of a few Watts are obtainable and these devices are being used in power amplifiers for transmitter driver chains and for point to point communications.

Work on monolithic microwave circuits which consist of FET devices and their associated matching circuitry all defined on a single chip of GaAs is currently at the research stage. This technique which offers small size and potential cost advantages is being studied both for receiver (low noise) and transmitter (power) applications in phased array systems where large numbers of similar circuits are required.
The research into GaAs integrated circuits is aimed at utilising the high frequency advantages of the material to realise circuits, both digital and linear, which will operate at frequencies above the limit of present silicon devices. Further development of the low noise FET have resulted in increased frequencies of operation and improved noise performance. The dual gate GaAs FET pioneered by Turner (48,49) has been refined and with one micron length gates is now capable of operation to above 12GHz.

To enable these new devices to be incorporated into microwave components (amplifiers, oscillators, mixers) developments have taken place in circuit design and realisation to cope with the particular characteristics of FETs. Computer Aided Design (CAD) programmes are now available which allow circuit optimisation for noise figure as well as gain performance and will take account of microstrip circuit effects such as dispersion which become significant at the higher operating frequencies of the FET.

Circuit techniques capable of matching the high impedances of low noise devices over broad bandwidths now exist and methods of achieving a good noise figure match with minimum loss are being sought. Indeed at frequencies below about 4GHz because the intrinsic noise figure of GaAs FETs is so good ($<$ 1dB typically for half micron gate lengths) significant improvements in amplifier performance is now resulting from reducing circuit losses rather than looking for better devices.

Small signal and power GaAs FETs in various amplifier and oscillator circuits are now established components in many microwave systems, both military and commercial. The dual gate FET is being used for gain control, mixer and modulator applications. The impact of monolithic and GaAs integrated circuits on microwave systems has yet to be seen, but it is interesting to remember, when considering the situation today, that it has been less than ten years since Plessey put the first ever commercial GaAs FET onto the market.

8.6. Recommendations

The on-line computer corrected network analyser system at Warwick, while capable of good results, does have some scope for improvement and further development. Higher measurement accuracy could be obtained by improving the setting accuracy of the microwave source frequency as discussed in section 8.2. An increase in dynamic range when measuring amplifiers could be obtained by utilising the switchable attenuator in the s-parameter test set. There is also a small further accuracy improvement to be gained by considering imperfections in the operation of the microwave sampling head and output display unit.

As a result of the dramatic plunge in the cost of computer systems and memory devices it would now be feasible to replace the on-line Sigma V computer with a microcomputer system dedicated for operation with the network analyser. This would have the advantage of removing limitations on the operation of the system due to problems of access time to the Sigma V. A suitable microcomputer with adequate computing and controlling power can now be purchased for a few thousand pounds which could readily be interfaced to the existing microwave system. If necessary this dedicated system could still be linked to the Sigma V for additional processing, storage or the display of data. With the broadening interest in GaAs based devices there are many possible topics for further research. Most prime parameters (i.e. gain, noise figure, output power) are however being investigated to varying extents, by the companies and research establishments concerned with the development of these new devices. Consideration of secondary topics may be more suited to continuing university research projects, such as investigations of performance stability, light sensitivity, overload characteristics and reliability. The ultimate importance of secondary device parameters is illustrated by the present situation with the established low noise small signal GaAs FETs where performance stability is causing problems in amplifiers requiring precise levels of gain under varying operating conditions.

In order to satisfy this requirement it has been necessary to carry out additional device research to overcome effects neglected when the device was first developed.

There are numerous applications of these GaAs devices, which although reports appear in the literature, are still only partially understood and could benefit from further investigation. Some examples are FET mixers, power oscillators and optoelectronic circuits together with techniques such as low loss matching and high frequency microstrip circuit realisation.

When considering fruitful topics of further research it should perhaps be remembered however, that the devices considered above all depend for their existance on Gallium Arsenide, a material which itself is far from being completely understood. There are thus still many continuing areas of materials research and only with success in these areas, leading to improved availability of high quality GaAs, will the realisation of future sophisticated devices be possible.

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APPENDIX 1. Two port correction programme listing.

The following listing, included for reference by others wishing to use the Warwick facility, is of the final programme used to affect full correction 2-port measurements without the need to manually reverse the device under test.

Written in Fortran IV and run on the Sigma V computer this programme controls the microwave equipment and the measurement of data via the interface units described (Ch. III).

This programme also contains subroutines to record results onto magnetic tape and retrieve them as well as routines to calculate and print gain and stability parameters.

```
      SUBROUTINE ONE
      IMPLICIT COMPLEX(S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
     2,CL2,ICA2,MPRT,PAD(18)
      COMMON ICOM(20)
      COMMON S(50,26)
      COMMON/PROUSET/LCOUNT,MAGMKR,NEND,NOCAL,KMKR,LMKR
      COMMON/TAPE/NTITLE(2),NTAPE,NAR,NCOM,NDATE(4),NS,NF,NPOINT
      COMMON/ITEXS/ITEXY(9,19)
      DATA ITEXY/
     1'K=1   CONNECT MA','TCHED LOAD ON PO','RT 1',
     2'K=2   SLIDE LOAD','                ',',    ',
     3'K=3   SLIDE LOAD','                ',',    ',
     4'K=4   SLIDE LOAD','                ',',    ',
     5'K=5   CONNECT MA','TCHED LOAD ON PO','RT 2',
     6'K=6   SLIDE LOAD',',               ',',    ',
     7'K=7   SLIDE LOAD',',               ',',    ',
     8'K=8   SLIDE LOAD',',               ',',    ',
     9'K=9   FWD TRANSM',',  2 MATCHED LOAD','S   ',
     A'K=10  REV TRANSM',',  2 MATCHED LOAD','S   ',
     B'K=11  SHORT CIRC','UIT ON PORT 1   ',',    ',
     C'K=12  OFFSET SHO','RT 1 ON PORT 2  ',',    ',
     D'K=13  SHORT CIRC','UIT ON PORT 2   ',',    ',
     E'K=14  OFFSET SHO','RT 1 ON PORT 1  ',',    ',
     F'K=15  CONNECT TH','ROUGH LINE      ',',    ',
     G'                ',',               ',',    ',
     H'                ',',               ',',    ',
     I'                ',',               ',',    ',
     J'K=19  CONNECT DE','VICE            ',',    '/
         DATA NPUSH/1/,I/0/
C
C     INITIALISATION
C
      LCOUNT=0
      CALL COCINIT(2)
      CALL FGDTEMP(100)
      CALL PRERLS(509,2Z69)
      CALL SEGLOAD(4)
1     CALL INITIAL
      IF(K)25,25,4
4     CALL SEGLOAD(1)
      CALL SEG1(NPUSH)
      GO TO(10,15,20,25,30)NPUSH
10    RETURN
C
C     DUMP RESULTS ON DISC
C
15    CALL SEGLOAD(4)
      CALL SEGLOAD(44)
      CALL PRSPOOL
      GO TO 3
C
C     DISPLAY RESULTS
C
20    CALL SEGLOAD(3)
      CALL DISPLAY
      GO TO 3
C
C     TASK
C
25    CALL SEGLOAD(4)
26    CALL TASK(I)
```

```
      GO TO(3,1,20,25,40,40)I
      GO TO 25
C
C     DUMP RESULTS
C
30    CALL SEGLOAD(4)
      CALL SEGLOAD(43)
      CALL DUMPER
      GO TO 3
C
C     PRINT RESULTS FROM DISC
C
42    CALL SEGLOAD(4)
      CALL SEGLOAD(44)
      CALL DESPOOL
      CALL SEGLOAD(6)
      CALL PRINS
      LCOUNT=LCOUNT-1
40    IF(LCOUNT)25,25,42
C
C     PROGRAM RELEASE PROCEDURE
C
50    I=7
      GO TO 25
      END


      SUBROUTINE RESET
      IMPLICIT COMPLEX (S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,BEN
     2,PAD(23)
      CONTINUE
      S     LW,10      =8Z80000000
      S     WD,10      X'C228'
      DO 1 KL=1,40000
    1 CONTINUE
      S     LI,10      0
      S     WD,10      X'C228'
      DO 2 KL=1,40000
    2 CONTINUE
      CALL FCHANG(LOW)
      END


      SUBROUTINE FCHANG(KS)
      DO 3 I=1,KS
      CALL PULSE
    3 CONTINUE
      CALL RDAC(2,10.0)
      CALL RDAC(2,10.0,2,10.0,2,-2.0)
      END


      FUNCTION CANG(ST)
      COMPLEX ST
      REAL RD
      DATA RD/57.29578/
      D1=AIMAG(ST)
      D2=REAL(ST)
      IF(D1+D2)4,2,4
    2 CANG=0.0
      RETURN
```

```
      C     RD IS 180.0/PI  =  CONVERTS RADIANS TO DEGREES
      4     CANG=RD*ATAN2(D1,D2)
            END

            SUBROUTINE SEG1(NPUSH)
            IMPLICIT COMPLEX (S)
            COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOP,LOW,NOZ,
           1KJGY,LL,II,IA,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,DEN
           2,PAD(23)
            COMMON ICOM(20)
            COMMON S(50,26)
            COMMON/ITEXS/ITEXY(9,19)
            DIMENSION ASA(22)
            DATA ASA/4*0.0,4*7.0,4*0,10.0,0*0,7.0,7*0,0*0,0*0,4*0,/*0,1*0,0,0*0
           1,4*0,7*0,10.0/
            CALL SEGLOAD(12)
            GO TO(5,21,23,13,13)NPUSH
            GO TO 13
      C
      C     START MEASURING
      C
      5     CALL RESET
            CALL RDAC(3,ASA(K))
            IF(K.EQ.19)GO TO 7
            IF(K.GT.15)GO TO 9
      7     CALL WT(36,ITEXY(1,K))
            CALL CHOOSE(1,'>',1,'YES,NO;',I)
            CALL WTNL
            GO TO(9,25)I
            GO TO 7
      9     CONTINUE
            IF(K.EQ.4.OR.K.EQ.8)GO TO 10
            II=0
            IT=0
            CALL ENAB(2Z63)
            CALL WAIT
            CALL DISAB(2Z63)
      10    K=K+1
      13    IF(K)25,25,11
      11    IF(K-19)5,15,14
      14    IF(K-23)5,20,20
      C
      C     CALIBRATION READINGS MADE
      C     READY FOR NEW DEVICE
      C
      15    CALL WTNL
            CALL CHOOSE(14,'NEW DEVICE ? >',1,'YES,NO;',I)
            GO TO(16,25)I
            GO TO 15
      16    DO 17 I=1,20
      17    IARRAY(I)=8Z4040404040
            CALL WTNL
            CALL WTNL(46,'TYPE DEVICE IDENTIFICATION & TERMINATE WITH CR')
            IBC=-80
            CALL RDNL(IBC,IARRAY)
            GO TO 5
      C
      C     UNKNOWN DEVICE READINGS MADE
      C     CALIBRATE AND COMPUTE
      C
      20    K=19
            CALL SEGLOAD(11)
```

```
      CALL CALC
      NPUSH=2
      RETURN
21    CALL WTNL
      CALL WT(39,'IS VDU DISPLAY REQUIRED ? (TYPE Y OR N)')
      CALL CHOOSE(1,'!',1,'YES,NO;',I)
      CALL WTNL
      GO TO(22,23)I
      GO TO 21
22    NPUSH=3
      RETURN
23    CALL WT(41,'DATA TO BE DUMPED ON TAPE ? (TYPE Y OR N)')
      CALL CHOOSE(2,' !',1,'YES,NO;',I)
      CALL WTNL
      GO TO(24,13)I
      GO TO 23
24    NPUSH=5
      RETURN
25    NPUSH=4
      RETURN
      END

       SUBROUTINE CALC
      IMPLICIT COMPLEX(S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
     2,CL2,ICA2,MPRT,PAD(18)
      COMMON ICOM(20)
      COMMON S(50,26)
      DATA C/2.9977E+10/
      DATA PI/3.1415927/
      SUN=(1.0,0.0)
      DO 100 I=1,NOF
      F=FMIN+(I-1)*FINC
      C1=2.*PI*F*CL1/C
      SL1=CMPLX(COS(-C1),SIN(-C1))
      SL2=CMPLX(COS(-2.*C2),SIN(-2.*C2))
      IF(ITYP-1)2,2,20
2     CONTINUE
C     WAVEGUIDE
20    A1=4.0*PI*F*CA1/C
      SA1=-SUN*CMPLX(COS(-A1),SIN(-A1))
      A2=4.0*PI*F*CA2/C
      SA2=-SUN*CMPLX(COS(-A2),SIN(-A2))
      IF(ICA1-1)30,30,25
25    B1=4.0*PI*F*CB1/C
      SB1=-SUN*CMPLX(COS(-B1),SIN(-B1))
      GO TO 35
30    B1=2.*PI*F*CB1*ZERO
      B1=2.*ATAN(B1)
      SB1=CMPLX(COS(-B1),SIN(-B1))
35    IF(ICA2-1)45,45,40
40    B2=4.0*PI*F*CB2/C
      SB2=-SUN*CMPLX(COS(-B2),SIN(-B2))
      GO TO 50
45    B2=2.*PI*F*CB2*ZERO
      B2=2.*ATAN(B2)
      SB2=CMPLX(COS(-B2),SIN(-B2))
50    CALL SLIDE(S(I,1),S(I,2),S(I,3),S(I,4),SERO)
      CALL SLIDE(S(I,5),S(I,6),S(I,7),S(I,8),STERO)
      SERO=S(I,9)
      STERO=S(I,10)
```

```
      SX1=S(I,11)-SE00
      SX2=S(I,14)-SE00
      SX3=S(I,14)-S(I,11)
      SX4=S(I,15)-SE00
      SX5=S(I,16)-SE30
      STX1=S(I,13)-STE00
      STX2=S(I,12)-STE00
      STX3=S(I,12)-S(I,13)
      STX4=S(I,17)-STE00
      STX5=S(I,18)-STE30
      SE11=(SA1*SX2-SB1*SX1)/(SA1*SB1*SX3)
      SE01=(SX1*SX2*(SB1-SA1))/(SA1*SB1*SX3)
      SL22=SX4/(SL2*(SE01+SX4*SE11))
      SE32=(SX5*(SUN-SL2*SE11*SE22))/SL1
      STE11=(SA2*STX2-SB2*STX1)/(SA2*SB2*STX3)
      STE01=(STX1*STX2*(SB2-SA2))/(SA2*SB2*STX3)
      STE22=STX4/(SL2*(STE01+STX4*STE11))
      STE32=(STX5*(SUN-SL2*STE11*STE22))/SL1
      S(I,23)=S(I,19)
      S(I,24)=S(I,20)
      S(I,25)=S(I,21)
      S(I,26)=S(I,22)
      KN=10
      DO 100 KJ=1,KN
      SQ=S(I,24)*S(I,26)-S(I,23)*S(I,25)
      SD=SUN*(SE11*S(I,23)+SE22*S(I,25)+SE11*S(I,24)*SE22*S(I,26)-
     1SL11*S(I,23)*SE22*S(I,25))
      STD=SUN*(STE11*S(I,25)+STE22*S(I,23)+STE11*S(I,26)*STE22*S(I,24)
     .1-STE11*S(I,25)*STE22*S(I,23))
      S(I,23)=(S(I,19)-SE00)*SD/SE01-SE22*SQ
      S(I,24)=(S(I,20)-SE30)*SD/SE32
      S(I,25)=(S(I,21)-STE00)*STD/STE01-STE22*SQ
      S(I,26)=(S(I,22)-STE30)*STD/STE32
  100 CONTINUE
      END

      SUBROUTINE SLIDE(S1,S2,S3,S4,SML)
      IMPLICIT COMPLEX (S)
      SA=S1/2.0+S2/2.0
      SB=S1/2.0+S3/2.0
      AM=(REAL(S2)-REAL(S1))/(AIMAG(S1)-AIMAG(S2))
      AN=(REAL(S3)-REAL(S1))/(AIMAG(S1)-AIMAG(S3))
      X=(AIMAG(SB)-AIMAG(SA)+AM*REAL(SA)-AN*REAL(SB))/(AM-AN)
      Y=(REAL(SB)-REAL(SA)+(AIMAG(SA)/AM)-(AIMAG(SB)/AN))/(1.0/AM-1.0/AN
     1)
      SML=CMPLX(X,Y)
      SMT=(S1+S2+S3)/3.0
      XX=CABS(SML)
      YY=CABS(SMT)*1.5
      IF(XX.GT.YY)SML=SMT
      END

      SUBROUTINE RDATA
      IMPLICIT COMPLEX (S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOP,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,BEN
     2,PAD(23)
      COMMON ICOM(20)
      COMMON S(50,26)
      IT=IT+1
      IF(II.NE.0)GO TO 8
```

```
      IF(IT.LT.180)RETURN
      GO TO 9
    8 CONTINUE
      IF(IT.LT.IN)RETURN
    9 CONTINUE
      II=II+1
      IF(II.GT.NOF)GO TO 2
      CALL VOLT(ST)
      CALL FIX(ST)
      S(II,K)=ST
      F=FMIN+(II-1)*FINC
      FUP=12.0
      FF=(FMAX+FMIN)/1.0E+9
      IF(FF.LT.4.0)FUP=2.0
      IF(FF.GT.4.0.AND.FF.LT.8.0)FUP=4.0
      IF(FF.GT.8.0.AND.FF.LT.14.0)FUP=8.0
      FUP=FUP*1E+9
      KS=ICO(F+FINC)-ICO(F)
      IF((F+FINC).GT.FUP)KS=ICO(F)-ICO(F-FINC)
      IT=0
      CALL FCHANG(KS)
      RETURN
    2 CALL TRIGR(2269)
      END

      SUBROUTINE FIX(ST)
      IMPLICIT COMPLEX(S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,BEN
     2,PAD(23)
      IF(IBOX-2)1,2,3
    3 ST=ST-SCENT
      GO TO 5
    1 R=10.0**REAL(ST)
      GO TO 4
    2 R=REAL(ST)
    4 TH=3.141529*AIMAG(ST)/1.8
      X=R*COS(TH)
      Y=R*SIN(TH)
      ST=CMPLX(X,Y)
    5 CONTINUE
      END

      SUBROUTINE VOLT(ST)
      IMPLICIT COMPLEX(S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,BEN
     2,PAD(23)
      DIMENSION AR(2)
      DO 12 J=1,2
      ASUM=0.0
      DO 11 I=1,NOZ
   10 CALL RADCS(1,AR(J),10.0,J)
   11 ASUM=ASUM+AR(J)
      AR(J)=ASUM/NOZ
      IF(NAMP.EQ.1)AR(J)=AR(J)/6.45
   12 CONTINUE
      ST=CMPLX(AR(1),AR(2))
      END
```

```
      FUNCTION ICO(FRE)
      IMPLICIT COMPLEX(S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,BEN
     2,PAD(23)
      DIMENSION ICAL(110)
      DIMENSION MCAL(82)
      DIMENSION JCAL(38)
      DIMENSION KCAL(43)
      DATA JCAL/
     111490,13230,14963,16715,18445,20140,20260,23596,25356,27110,
     228848,30610,32340,34080,35823,37568,39310,41013,42775,44522,
     346272,48000,49733,51440,53215,54984,56726,58264,60010,62050,
     463779,65390,67210,69036,70830,72566,74147,76058/
      DATA KCAL/
     112935,4699,6445,8210,9970,11690,13451,15197,16931,18708,
     220456,22113,23910,25664,27402,29130,30778,32540,34300,36051,
     337790,39532,41274,43024,44745,46498,48247,49987,51651,53409,
     455173,56909,58677,60440,62190,63904,65668,67382,69110,70843,
     572609,74309,76107/
      DATA MCAL/
     112960,3784,4609,5527,6404,7381,8230,9127,10128,10961,
     211770,12531,13472,14340,15210,16146,17106,18040,18870,19660,
     320553,21439,22349,23240,24163,25179,25990,26884,27704,28561,
     429470,30384,31308,32253,33169,33986,34823,35674,36563,37448,
     538320,39241,40203,41072,41850,42677,43572,44421,45327,46197,
     647137,48078,48889,49699,50509,51388,52242,53122,54009,54909,
     755853,56681,57485,58309,59149,59999,60871,61740,62665,63606,
     864482,65283,66136,66973,67847,68685,69595,70535,71427,72309,
     973169,73967/
      DATA ICAL/
     112950,3552,4214,4759,5470,6138,6751,7447,8097,8741,
     229432,10092,10759,11385,12022,12677,13309,13954,14595,15237,
     315869,16542,17229,17884,18539,19172,19807,20429,21043,21658,
     422336,23003,23691,24421,25080,25675,26300,26906,27497,28159,
     528805,29446,30200,30873,31525,32210,32799,33388,34069,34661,
     635285,36008,36647,37299,38000,38657,39345,39969,40581,41239,
     741886,42528,43194,43823,44472,45139,45711,46484,47156,47789,
     848431,49068,49688,50323,50928,51599,52247,52900,53609,54295,
     954920,55558,56164,56785,57421,58056,58720,59370,60023,60710,
     A61375,62059,62670,63269,63900,64531,65173,65822,66470,67137,
     867790,68453,69120,69776,70426,71052,71690,72352,72976,73652/
      FSTART=7.0
      F=(FMAX+FMIN)/1.0E+9
      IF(F.LT.4.0)FSTART=0.25
      IF(F.GT.4.0.AND.F.LT.8.0)FSTART=2.0
      IF(F.GT.8.0.AND.F.LT.14.0)FSTART=4.0
      FRE=FRE/1.0E+9
      J=(FRE-FSTART)*20.0
      FCAL=FSTART+J*0.05
      FCAL=FCAL*1.0E+9
      FRE=FRE*1.0E+9
      J=J+2
      FDIFF=0.05*1.0E+9
      IF(FMAX+FMIN.GT.4.0E+9)GO TO 5
      ICO=(FRE-FCAL)*(JCAL(J)-JCAL(J-1)+0.0)/FDIFF+JCAL(J-1)
      RETURN
    5 CONTINUE
      IF(FMAX+FMIN.GT.8.0E+9)GO TO 6
      ICO=(FRE-FCAL)*(KCAL(J)-KCAL(J-1)+0.0)/FDIFF+KCAL(J-1)
      RETURN
    6 CONTINUE
      IF(FMAX+FMIN.GT.14.0E+9)GO TO 7
```

```
      ICO=(FRE-FCAL)*(MCAL(J)-MCAL(J-1)+0.0)/FDIFF+MCAL(J-1)
      RETURN
    7 CONTINUE
      ICO=(FRE-FCAL)*(ICAL(J)-ICAL(J-1)+0.0)/FDIFF+ICAL(J-1)
      END

      SUBROUTINE PRINS
      IMPLICIT COMPLEX (S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
     2,CL2,ICA2,MPRT,PAD(18)
      COMMON ICOM(20)
      COMMON S(50,26)
      DIMENSION XP(4),YP(4)
      WRITE(109,5)ICOM,IARRAY
    5 FORMAT(/1X,20A4/1H1,20A4///1X,
     1'FREQUENCY',10X,'S11',18X,'S12',18X,'S21',18X,'S22'/3X,
     2'GHZ',9X,4('AMP',6X,'PHASE',7X)/)
      DO 12 I=1,NOF
      F=(FMIN+(I-1)*FINC)/1.0E9
      DO 10 J=23,26
      XP(J-22)=CABS(S(I,J))
   10 YP(J-22)=CANG(S(I,J))
   12 WRITE(109,14)F,XP(1),YP(1),XP(4),YP(4),XP(2),YP(2),XP(3),YP(3)
   14 FORMAT(1X,F7.3,4(F12.3,F9.1))
      END

      SUBROUTINE DISPLAY
      IMPLICIT COMPLEX(S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
     2,CL2,ICA2,MPRT,PAD(18)
      COMMON ICOM(20)
      COMMON S(50,26)
      DIMENSION IV(8),IDY(5)
      DATA K1,K2/50,26/
      DATA IV/'U11','U21','U22','U12','S11','S21','S22','S12'/
  166 CONTINUE
   10 CALL TITLE(1,' ')
      CALL WTNL(19,'DISPLAY REQUIRED ? ')
      CALL WTNL(26,'AM  AMPLITUDE VS FREQUENCY')
      CALL WTNL(22,'PH  PHASE VS FREQUENCY')
      CALL WTNL(14,'PO  POLAR PLOT')
      CALL WTNL(33,'NO  NONE = LEAVE DISPLAY SEQUENCE')
      CALL CHOOSE(9,'PLOT ? !!',2,'AMPLITUDE,PHASE,POLAR,NONE;',JJ)
      CALL WTNL
      IF(JJ.EQ.4)RETURN
      IF(JJ.EQ.0)GO TO 10
      GO TO (1,2,3)JJ
    3 TX=300.0
      TY=300.0
      POSX=-1.0
      POSY=-1.0
      RX=2.0
      RY=2.0
      GO TO 6
    1 RY=1.0
      POSY=0.0
      TY=600.0/RY
      GO TO 5
    2 POSY=-180.0
```

```
      RY=360.0
      TY=600.0/RY
    5 RX=(FMAX-FMIN)/1.0E9
      TX=800.0/RX
      POSX=FMIN/1.0E9
    6 CALL WTML(18,'TERMINATE WITH CR ')
      CALL WT(26,'PARAMETERS TO BE PLOTTED  ')
      DO 33 J=1,5
      IBC=-3
      CALL RD(IBC,IDY(J))
      IF(IBC.EQ.0)GO TO 66
      DO 32 J2=1,8
      IF(IDY(J).EQ.IV(J2))GO TO 33
   32 CONTINUE
      GO TO 166
   33 CONTINUE
   66 J=J-1
      IF(J.EQ.0)RETURN
   14 CONTINUE
      CALL TITLE(80,IARRAY)
      CALL SEGLOAD(31)
       CALL SCALE(100.0,100.0,TX,TY)
      CALL AXIS(POSX,POSY,RX/5,RY/5,RX,RY)
      CALL SEGLOAD(32)
      DO 13 JK=1,J
      DO 11 JL=1,8
      IF(IDY(JK).EQ.IV(JL))GO TO 7
   11 CONTINUE
      GO TO 13
    7 X=(JK-1)*60
      Y=40.
      CALL TPLOT(0,X,Y)
      CALL ALPHA
      CALL WT(4,IV(JL))
   22 KP=18+JL
      GO TO (111,112,113)JJ
  111 Y=CABS(S(1,KP))
      GO TO 114
  112 Y=CANG(S(1,KP))
  114 X=FMIN/1.0E9
      GO TO 116
  113 Y= AIMAG(S(1,KP))
      X=REAL(S(1,KP))
  116 CALL GPLOT(X,Y,0,0,1)
      IL=-1
      IF(JL.LE.4)IL=1
      IM=JL
      IF(JL.GT.4)IM=JL-4
      DO 70 I=1,NOF
      GO TO (211,212,213)JJ
  211 Y=CABS(S(1,KP))
      GO TO 214
  212 Y=CANG(S(1,KP))
  214 X=(FMIN+(I-1)*FINC)/1.0E9
      GO TO 216
  213 Y= AIMAG(S(I,KP))
      X=REAL(S(I,KP))
  216 CALL GPLOT(X,Y,IL,IM,1)
   70 CONTINUE
   13 CONTINUE
      IF(KJOY.NE.1)GO TO 667
      CALL JOY(ICHAR,IX,IY)
      IF(ICHAR.EQ.8ZD9040400)GO TO 166
```

```
538            BX=POSX
539            BY=POSY
540            POSX=FLOAT(IX-100)/TX+BX
541            POSY=FLOAT(IY-100)/TY+BY
542            CALL JOY(ICHAR,IX,IY)
543            IF(ICHAR.EQ.8ZD9404040)GO TO 166
544            EGX=FLOAT(IX-100)/TX+BX
545            EGY=FLOAT(IY-100)/TY+BY
546            GO TO 67
547          667 CALL TPLOT(0,0,20)
548            CALL ALPHA
549            CALL WT (7,'MAX X =')
550            IBC=12
551            CALL RD(IBC,POSX)
552            IF(IBC.EQ.0)GO TO 10
553            CALL WT (7,'MIN X =')
554            IBC=12
555            CALL RD(IBC,EGX)
556            CALL WT (7,'MAX Y =')
557            IBC=12
558            CALL RD(IBC,POSY)
559            CALL WT (7,'MIN Y =')
560            IBC=12
561            CALL RD(IBC,EGY)
562           67 CONTINUE
563            TX=RX*TX/(ABS(POSX-EGX))
564            TY=RY*TY/(ABS(POSY-EGY))
565            RX=ABS(POSX-EGX)
566            RY=ABS(POSY-EGY)
567            IF(POSX.LT.EGX)GO TO 69
568            POSX=EGX
569           69 IF(POSY.LT.EGY)GO TO 64
570            POSY=EGY
571           64 GO TO 14
572            END

573            SUBROUTINE SCALE(XOFF,YOFF,SCALEX,SCALEY)
574            COMMON/SCAXPL/03,04,S3,S4,05,06,YS
575            S3=SCALEX
576            S4=SCALEY
577            03=XOFF
578            04=YOFF
579            RETURN
580            END

581            SUBROUTINE DEFALT
582            COMMON/SCAXPL/03,04,S3,S4,05,06,YS
583            03=100
584            04=100
585            S3=1
586            S4=1
587            05=0
588            06=0
589            YS=999999
590            RETURN
591            END

592            SUBROUTINE TASK(J)
593            IMPLICIT COMPLEX(6)
594            COMMON NFILE,IDATE(6),IARRAY(20),FMIN,FMAX,FINC,SCENT,NMF,LOW,IOZ,
```

```
     1*            1KJOY,LL,II,IA,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
     2*            2,CL2,ICA2,MPRT,PAD(18)
   597             COMMON ICOM(20)
   598             COMMON S(50,26)
     1*            COMMON/PROGSET/LCOUNT,MAGMKR,NEND,NOCAL,KMKR,LMKR
   600             COMMON/ITEXS/ITEXY(9,19)
     1*            GO TO(4,4,4,4,125,252,120)J
     2*      4     J=1
   603       1     CALL WTNL
   604             CALL WT(38,'TASK ? (TYPE LI FOR LIST OF OPTIONS)  ')
   605             CALL CHOOSE(2,'!!',2,'LI,ZE,BG,RE,SK,ND,CA,PR,DI,DU,UD,ST,CO,CE,AM
     1*           1,IN,WA,CL,JO,FR,MF,NO,TI,TF,DC,LT,UT;',I)
   607             IF(I)1,1,2
   608       2     CALL TITLE(1,' ')
   609             CALL SEGLOAD(41)
   610             GO TO(10,20,30,40,50,60,70,80,90,100,110,120,130,140,150,
   611            1160,170,180,190,200,210,220,230,240,250,260,270,280,290,300)I
   612             CALL WTNL(18,'UNRECOGNISABLE KEY')
   613             GO TO 1
   614       C
   615       C     LIST OPTIONS
   616       10    CALL WTNL(39,'TASK OPTIONS - TWO LETTER KEYS REQUIRED')
   617             CALL WTNL(50,'LI  LIST OPTIONS           ZE  RESTART PROGRAM    ')
   618             CALL WTNL(50,'BG  RESTART CALIBRATION    RE  REPEAT LAST READING')
   619             CALL WTNL(50,'SK  RESET K (SEE BELOW)    ND  GO TO NEW DEVICE   ')
   620             CALL WTNL(50,'CA  CALCULATE              PR  PRINT              ')
   621             CALL WTNL(50,'DI  ENTER DISPLAY          DU  DUMP READINGS      ')
   622             CALL WTNL(50,'UD  UNDUMP READINGS        ST  RELEASE PROGRAM    ')
   623             CALL WTNL(50,'CO  INSERT COMMENT         CE  CENTRE BEAM        ')
   624             CALL WTNL(50,'AM  RESET AMPLIFIERS       IN  RESET INPUT TYPE   ')
   625             CALL WTNL(50,'WA  WAVEGUIDE OR COAX      CL  DEFINE CALIB PIECES')
   626             CALL WTNL(50,'JO  JOYSTICK SWITCH        FR  RESET FREQ RANGE   ')
     1*            CALL WTNL(50,'MF  CORRECT MIN FREQ       NO  RESET NO. READINGS ')
   628             CALL WTNL(50,'TI  RESET TIMING INT       TF  UPDATE TAPE FORMAT ')
     1*            CALL WTNL(50,'DC  DISC FILE CLEAR        LT  LOAD DATA TAPE     ')
     2*            CALL WTNL(50,'UT  UNLOAD DATA TAPE                              ')
   631             CALL WTNL
   632             CALL WTNL
   633             CALL WTNL(27,'SETTINGS FOR K IN SK OPTION')
   634             DO 12 L=1,19
   635       12    CALL WTNL(36,ITEXY(1,L))
   636             J=4
   637             RETURN
   638       C
   639       C     RESTART PROGRAM
   640       20    CALL SEGLOAD(46)
   641             CALL TAPEEND
   642             J=2
   643             RETURN
   644       C
   645       C     RESTART CALIBRATION
   646       30    K=1
   647             RETURN
   648       C
   649       C     REPEAT LAST READING
   650       40    K=K-1
   651             IF(K.LT.1)K=1
   652             RETURN
   653       C
   654       C     RESET K
   655       50    DO 52 L=1,19
   656       52    CALL WTNL(36,ITEXY(1,L))
   657             CALL WTNL
```

```
658             IBC=2
659             CALL RDNL(31,'TERMINATION NO. REQUIRED ? K = ',IBC,K)
660             IF(K.GT.19)GO TO 50
661             IF(K.LE.0)GO TO 50
662             RETURN
663         C
664         C   GO TO NEW DEVICE
665         60  K=19
666             RETURN
667         C
668         C   CALCULATE
669         70  K=23
670             RETURN
671         C
672         C   PRINT
673         80  CALL SEGLOAD(44)
674         81  CALL PRSPOOL
675         86  RETURN
676         C
677         C   ENTER DISPLAY
678         90  J=3
679             RETURN
680         C
681         C   DUMP READINGS
682         100 CALL SEGLOAD(43)
683             CALL DUMPER
684             RETURN
685         C
686         C   UNDUMP READINGS
  1*        110 CALL SEGLOAD(46)
688             CALL UNDUMP
690             J=4
691             RETURN
692         C
693         C   RELEASE PROGRAM
  1*        120 IF(NEND)126,122,126
  2*        122 J=5
695             CALL SEGLOAD(46)
696             CALL TAPEEND
697         121 IF(LCOUNT.EQ.0)GO TO 129
698             CALL SEGLOAD(44)
699             CALL NEWSPOOL
700             CALL BACKWAIT
701         129 RETURN
702         125 CALL WTNL(15,'PROGRAM RELEASE')
  1*            NEND=1
  2*        126 CALL RELEASE
704             RETURN
705         C
706         C   INSERT COMMENT
707         130 CALL WTNL(32,'TYPE COMMENT & TERMINATE WITH CR')
708             IBC=-80
709             CALL RDNL(IBC,ICOM)
710             RETURN
711         C
712         C   CENTRE BEAM
713         140 CALL CENT
714             RETURN
715         C
716         C   RESET AMPLIFIERS
717         150 CALL AMP
718             RETURN
719         C
```

```
720         C     RESET INPUT TYPE
721         160   CALL BOX
722               RETURN
723         C
724         C     WAVEGUIDE OR COAX
725         170   L=ITYP
726               CALL WAVE
727               IF(ITYP.EQ.L)RETURN
728               CALL BOX
729               GO TO 200
730         C
731         C     DEFINE CALIB PIECES
732         180   CALL SEGLOAD(45)
733               CALL CALIB
734               RETURN
735         C
736         C     JOYSTICK SWITCH
737         190   CALL CHOOSE(43,'USE OF JOYSTICK REQUIRED ? (TYPE Y OR N) : ',1,
738              1'YES,NO;',L)
739               CALL WTNL
740               GO TO(192,192)L
741               GO TO 190
742         192   KJOY=L
743               RETURN
744         C
745         C     RESET FREQ RANGE
746         200   CALL SEGLOAD(42)
747               CALL FREQ
748               CALL MINSET
749               K=1
750               RETURN
751         C
752         C     CORRECT MIN FREQ
753         210   CALL SEGLOAD(42)
754               CALL MINSET
755               RETURN
756         C
757         C     RESET NO. POINTS
  1*        220   CALL WTNL(32,'NO. OF READINGS PER POINT NOW = ',NOZ)
759         222   IBC=2
  1*              CALL RDNL(27,'NO. OF READINGS REQUIRED = ',IBC,NOZ)
761               IF(NOZ)222,222,224
762         224   IF(NOZ.GT.50)GO TO 220
763               RETURN
764         C
765         C     RESET TIMING INT
766         230   CALL WTNL(35,'TIMING INTERVAL (N*0.01 SEC) NOW = ',IN)
767         232   IBC=4
768               CALL RDNL(40,'TIMING INTERVAL (N*0.01 SEC) REQUIRED = ',IN)
769               IF(IN.GT.500)GO TO 232
770               RETURN
771         C
772         C     CHANGE TAPE DUMP FORMAT FROM OLD TO NEW
773         240   CALL SHUFFLE
774               RETURN
775         C
776         C     DISC FILE CLEAR
777         250   J=6
778               GO TO 121
  1*        252   CALL SEGLOAD(44)
  2*              CALL NEWSPOOL
  3*              GO TO 4
779         C
```

```
  1*      260   CALL SEGLOAD(43)
  2*            MAGMKR=1
  3*            CALL TAPEGO
  4*            RETURN
781       C
  1*      270   CALL SEGLOAD(46)
  2*            CALL TAPEEND
  3*            MAGMKR=0
  4*            RETURN
783       C
784       280   RETURN
785       C
786       290   RETURN
787       C
788       300   RETURN
789             END


790             SUBROUTINE INITIAL
791             IMPLICIT COMPLEX(S)
792             COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOP,LOW,NOZ,
  1*           1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
  2*           2,CL2,ICA2,MPRT,PAD(18)
795             COMMON ICOM(20)
  1*            COMMON/PROGSET/LCOUNT,MAGMKR,NEND,NOCAL,KMKR,LMKR
  2*            CALL RDAC(1,0.0,2,-2.0,3,0.0,4,0.0,5,0.0)
797             CALL TITLE(31,'2-PORT FULL CORRECTION PROGRAM.')
  1*            CALL WTNL(13,'VERSION 6L2/3')
  2*            NEND=0
799             K=0
800             DO 4 L=1,20
801       4     ICOM(L)=8Z4040404040
802       1     CALL WT(37,'INITIALISATION REQUIRED ? TYPE Y OR N')
803             CALL CHOOSE(2,' >',1,'YES,NO;',I)
804             CALL WTNL
  1*            GO TO(5,5)I
  2*            GO TO 1
  3*      5     CALL WT(39,'USE OF DATA TAPE REQUIRED ? TYPE Y OR N')
  4*            CALL CHOOSE(2,' >',1,'YES,NO;',L)
  5*            CALL WTNL
  6*            MAGMKR=L
  7*            IF(L.EQ.2)MAGMKR=0
  8*            GO TO(6,7)L
  9*            GO TO 5
 10*      6     CALL SEGLOAD(43)
806             CALL TAPEGO
  1*      7     GO TO(2,3)I
808             GO TO 1
809       2     CALL SEGLOAD(41)
811             CALL AMP
812             CALL WAVE
813             CALL SEGLOAD(45)
814             CALL CALIB
815             CALL WTNL(23,'JOYSTICK IS NOT IN USE.')
816             KJOY=2
  1*            CALL WTNL(29,'NO. OF READINGS PER POINT =10')
818             NOZ=10
819             CALL WTNL(35,'TIMING INTERVAL ( N*0.01 SEC). N=30')
820             I=30
821             CALL SEGLOAD(41)
822             CALL BOX
823             CALL SEGLOAD(42)
824             CALL FREQ
```

```
      CALL MINSET
      K=1
      CALL TITLE(1,' ')
    3 RETURN
      END


      SUBROUTINE CALIB
      IMPLICIT COMPLEX(S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
     2,CL2,ICA2,MPRT,PAD(18)
      COMMON/ITEXS/ITEXY(9,19)
      DIMENSION ISUBS(8,10)
      DATA ISUBS/
     1'      OFFSET SHO','RT 1 ON PORT 1  ',
     2'      OFFSET SHO','RT 1 ON PORT 2  ',
     3'      OPEN CIRCU','IT ON PORT 2    ',
     4'      OPEN CIRCU','IT ON PORT 1    ',
     5'      OFFSET SHO','RT 2 ON PORT 2  ',
     6'      OFFSET SHO','RT 2 ON PORT 1  ',
     7'      SHORT CIRC','UIT ON PORT 1   ',
     8'      SHORT CIRC','UIT ON PORT 2   ',
     9'      OFFSET SHO','RT 3 ON PORT 2  ',
     A'      OFFSET SHO','RT 4 ON PORT 2  '/
      CALL WTNL
      CALL WTNL(63,'STANDARD CALIBRATION USES SLIDING LOAD, SHORT AND OF
     1FSET SHORT.')
    2 CALL CHOOSE(48,'STANDARD CALIBRATION REQUIRED ? (TYPE Y OR NO) !',
     11,'YES,NO!',J)
      CALL WTNL
      IF(J-1)2,4,10
    4 CA1=0.0
      CA2=0.0
      ICA1=2
      ICA2=2
      CL1=0.0
      CL2=0.0
      DO 5 J=2,8
      ITEXY(J,11)=ISUBS(J,7)
      ITEXY(J,12)=ISUBS(J,2)
      ITEXY(J,13)=ISUBS(J,8)
    5 ITEXY(J,14)=ISUBS(J,1)
    6 IBC=8
      CALL RDNL(30,'LENGTH OF OFFSET SHORT (CM) = ',IBC,CB1)
      IF(CB1)7,6,7
    7 CB2=CB1
      RETURN
   10 CALL WTNL
      CALL WTNL(36,'CALIBRATION PIECE 1 IS MATCHED LOAD.')
      CALL WTNL(45,'CALIB. PIECE 2 CAN BE SHORT OR OFFSET SHORT.')
      CALL WTNL(51,'CALIB. PIECE 3 CAN BE OPEN CIRCUIT OR OFFSET SHORT.
     1')
      CALL WTNL(31,'CALIB. PIECE 4 IS THROUGH LINE.')
      CALL WTNL
      LOFFS=0
C
C     PORT 1 CALIB PIECE 2
C
   12 CALL CHOOSE(42,'PORT 1: CALIB PIECE 2 ? (TYPE SH OR OF) !!',2,'SHO
     1RT,OFFSET;',J)
      CALL WTNL
      IF(J-1)12,20,15
```

```
C     OFFSET SHORT
15    DO 17 J=2,8
17    ITEXY(J,11)=ISUBS(J,1)
      LOFFS=LOFFS+1
19    IBC=8
      CALL RDNL(30,'LENGTH OF OFFSET SHORT (CM) = ',IBC,CA1)
      IF(CA1)22,19,22
C     SHORT
20    CA1=0.0
      DO 21 J=2,8
21    ITEXY(J,11)=ISUBS(J,7)
C
C     PORT 1 CALIB PIECE 3
C
22    CALL CHOOSE(42,'PORT 1: CALIB PIECE 3 ? (TYPE OP OR OF) !!',2,'OPE
     1N,OFFSET)',J)
      CALL WTNL
      IF(J-1)22,30,24
C     OFFSET SHORT
24    ICA1=2
      LOFFS=LOFFS+1
      GO TO(27,25)LOFFS
25    DO 26 J=2,8
26    ITEXY(J,14)=ISUBS(J,6)
      GO TO 29
27    DO 28 J=2,8
28    ITEXY(J,14)=ISUBS(J,1)
29    IBC=8
      CALL RDNL(30,'LENGTH OF OFFSET SHORT (CM) = ',IBC,CB1)
      IF(CB1)72,29,72
72    IF(CB1-CA1)34,29,34
C     OPEN
30    ICA1=1
      DO 32 J=2,8
32    ITEXY(J,14)=ISUBS(J,4)
      IBC=8
      CALL RDNL(34,'CHARACTERISTIC IMPEDANCE (OHMS) = ',IBC,ZEDO)
      IBC=8
      CALL RDNL(33,'DISCONTINUITY CAPACITANCE (PF) = ',IBC,CB1)
      CB1=CB1*1.0E-12
C
C     PORT 2 CALIB PIECE 2
C
34    CALL CHOOSE(42,'PORT 2: CALIB PIECE 2 ? (TYPE SH OR OF) !!',2,'SHO
     1RT,OFFSET)',J)
      CALL WTNL
      IF(J-1)34,42,75
C     OFFSET SHORT
75    LOFFS=LOFFS+1
      GO TO(37,79,77)LOFFS
77    DO 78 J=2,8
78    ITEXY(J,13)=ISUBS(J,9)
      GO TO 41
79    DO 80 J=2,8
80    ITEXY(J,13)=ISUBS(J,5)
      GO TO 41
37    DO 39 J=2,8
39    ITEXY(J,13)=ISUBS(J,2)
41    IBC=8
      CALL RDNL(30,'LENGTH OF OFFSET SHORT (CM) = ',IBC,CA2)
      IF(CA2)44,41,44
C     SHORT
42    CA2=0.0
```

```
      DO 43 J=2,8
43    ITEXY(J,13)=ISUBS(J,8)
C
C     PORT 2 CALIB PIECE 3
C
44    CALL CHOOSE(42,'PORT 2: CALIB PIECE 3 ? (TYPE OP OR OF) !!',2,'OPE
     1N,OFFSET;',J)
      CALL WTNL
      IF(J-1)44,54,46
C     OFFSET SHORT
46    ICA2=2
      LOFFS=LOFFS+1
      GO TO(49,47,84,82)LOFFS
82    DO 83 J=2,8
83    ITEXY(J,12)=ISUBS(J,10)
      GO TO 51
84    DO 85 J=2,8
85    ITEXY(J,12)=ISUBS(J,9)
      GO TO 51
47    DO 48 J=2,8
48    ITEXY(J,12)=ISUBS(J,5)
      GO TO 51
49    DO 50 J=2,8
50    ITEXY(J,12)=ISUBS(J,2)
51    IBC=8
      CALL RDNL(30,'LENGTH OF OFFSET SHORT (CM) = ',IBC,C82)
      IF(C82)86,51,86
86    IF(C82-CA2)70,51,70
C     OPEN
54    ICA2=1
      DO 56 J=2,8
56    ITEXY(J,12)=ISUBS(J,3)
      IF(ICA1-1)58,60,58
58    IBC=8
      CALL RDNL(34,'CHARACTERISTIC IMPEDANCE (OHMS) = ',IBC,ZEDO)
60    IBC=8
      CALL RDNL(33,'DISCONTINUITY CAPACITANCE (PF) = ',IBC,C82)
      C82=C82*1.0E-12
C     THROUGH LINE
70    IBC=8
      CALL RDNL(41,'LENGTH OF THROUGH LINE CONNECTION (CM) = ',IBC,CL1)
      CL2=CL1
      RETURN
      END

      SUBROUTINE WAVE
      IMPLICIT COMPLEX(S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOP,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZEDO,OEN
     2,PAD(23)
    1 CALL WT  (32,'WAVEGUIDE OR COAX = TYPE W OR C')
      CALL CHOOSE(2,' !',1,'WAVEGUIDE,COAX;',I)
      CALL WTNL
      GO TO(2,2)I
      GO TO 1
2     ITYP=I
      END

      SUBROUTINE SHUFFLE
      IMPLICIT COMPLEX (S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOP,LOW,NOZ,
```

```
1KJOY,LL,II,IA,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZEDO,CA1,CL1,CA2,CB2
2,CL2,ICA2,MPRT,PAD(18)
 COMMON ICOM(20)
 COMMON S(50,26)
 IF(ICA1.EQ.2)GO TO 5
 CA1=0.
 CA2=0.
 CB2=CB1
 ICA1=2
 ICA2=2
 CL2=CL1
 RETURN
5  DO 10 I=1,NOF
 SS=S(I,11)
 S(I,11)=S(I,14)
 S(I,14)=SS
 SS=S(I,12)
 S(I,12)=S(I,13)
10  S(I,13)=SS
 CB2=CA1
 CA2=CB1
 CA1=CA2
 CB1=CB2
 ICA1=1
 ICA2=1
 CL2=CL1
 END

 SUBROUTINE APP
 IMPLICIT COMPLEX(S)
 COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
1KJOY,LL,II,IA,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZEDO,BEA
2,PAD(23)
1  CALL CHOOSE(37,'ARE AMPLIFIERS IN USE ? TYPE Y OR N !',1,'YES,NO;'
1,I)
 CALL WTNL
 GO TO(2,2)I
 GO TO1
2 NAMP=1
 END

 SUBROUTINE CENT
 IMPLICIT COMPLEX(S)
 COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
1KJOY,LL,II,IA,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZEDO,BEA
2,PAD(23)
 IF(IBOX.NE.3)GO TO 3
 IBC=-1
 CALL RDNL(39,'CENTRE BEAM WHILE TYPING ANY CHARACTER ',IBC,A)
 CALL VOLT(ST)
 SCENT=ST
 GO TO 4
3 CALL WTNL(23,'BEAM CENTRING NOT REQD.')
4  CONTINUE
 END

 SUBROUTINE VOLT(ST)
 IMPLICIT COMPLEX(S)
 COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
1KJOY,LL,II,IA,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZEDO,BEA
```

```
      2,PAD(23)
       DIMENSION AR(2)
       CALL RADCS(2,AR,10.0,1)
       DO 12 J=1,2
       ACK=ABS(AR(J))
       ASUM=0.0
       DO 11 I=1,NOZ
       CALL RADCS(1, AR(J),ACK,J)
   11  ASUM=ASUM+AR(J)
       AR(J)=ASUM/NOZ
       IF(NAMP.EQ.1)AR(J)=AR(J)/6.45
   12  CONTINUE
       S1=CMPLX(AR(1),AR(2))
       END


       SUBROUTINE BOX
       IMPLICIT COMPLEX(S)
       COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
      1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,BEN
      2,PAD(23)
     1 CALL WTNL(53,'INPUTS TAKEN FROM POLAR DISPLAY OR PHASE GAIN UNIT ?
      1 ')
       CALL CHOOSE(25,'TYPE LOG,LIN,OR POL !!!',3,'LOG,LIN,POL',1)
       CALL WTNL
       IBOX=I
       GO TO (2,2,3)I
       GO TO 1
     3 CALL CENT
     2 RETURN
       END


       SUBROUTINE MINSET
       IMPLICIT COMPLEX(S)
       COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
      1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,BEN
      2,PAD(23)
       CALL WTNL(24,'MINIMUM FREQUENCY SET UP')
     3 CALL RESET
       IBC=12
       CALL RDNL(29,'CORRECTION TO FREQ. IN MHZ = ',IBC,AMEG)
       IF(AMEG.EQ.0.0)GO TO 4
       LOW=LOW+AMEG*13.0
       IF(LOW.LE.0)LOW=1
       GO TO 3
    4  CONTINUE
       END


       SUBROUTINE FREQ
       IMPLICIT COMPLEX(S)
       COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
      1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,BEN
      2,PAD(23)
     1 IBC=12
       CALL RDNL(26,'MAXIMUM FREQUENCY (GHZ) = ',IBC,FMAX)
       IBC=12
       CALL RDNL(26,'MINIMUM FREQUENCY (GHZ) = ',IBC,FMIN)
       IF(FMAX.LT.FMIN)GO TO 1
       IF(FMAX.LT.12.1.AND.FMIN.GT.6.9)GO TO 8
       IF(FMAX.LT.8.1.AND.FMIN.GT.3.9)GO TO 8
       IF(FMAX.LT.4.1.AND.FMIN.GT.1.9)GO TO 8
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```
1122              IF(FMAX.LT.2.1.AND.FMIN.GT.0.05)GO TO 8
1123              GO TO 1
1124        8     CONTINUE
1125              FMIN=FMIN*1.0E9
1126              FMAX=FMAX*1.0E9
1127            2 IBC=2
1128              CALL RDNL(16,'NO. OF POINTS = ',IBC,NOF)
1129              IF(NOF.GT.50.OR.NOF.LT.2)GO TO 2
1130              FINC=(FMAX-FMIN)/(NOF-1.0)
1131              F=FMIN/1.0E9
1132              VOL=7.5
   1*             IF(F.LT.6.99)VOL=5.0
1134              IF(F.LT.4.0)VOL=3.0
1135              IF(F.LT.2.0)VOL=1.5
1136              CALL RDAC(4,VOL)
1137              LOW=ICO(FMIN)-3000
1138            5 CALL WTNL(25,'SWITCH TOLEC RESET TO 3V.')
1139            6 CONTINUE
1140              END


1141              FUNCTION ICO(FRE)
1142              IMPLICIT COMPLEX(S)
1143              COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
1144             1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CAL1,CAL2,ITYP,ICA,ZERO,BEN
1145             2,PAD(23)
1146              DIMENSION ICAL(110)
1147              DIMENSION MCAL(82)
1148              DIMENSION JCAL(38)
1149              DIMENSION KCAL(43)
1150              DATA JCAL/
1151             111490,13230,14963,16715,18445,20140,20260,23596,25356,27110,
1152             228848,30610,32340,34080,35823,37568,39310,41013,42775,44522,
1153             346272,48000,49733,51440,53215,54984,56726,58264,60010,62050,
1154             463779,65390,67210,69036,70830,72566,74147,76058/
1155              DATA KCAL/
1156             12935,4699,6445,8210,9970,11690,13451,15197,16931,18708,
1157             220456,22113,23910,25664,27402,29130,30778,32540,34300,36051,
1158             337790,39532,41274,43024,44745,46498,48247,49987,51651,53409,
1159             455173,56909,58677,60440,62190,63904,65668,67382,69110,70843,
1160             572609,74309,76107/
1161              DATA MCAL/
1162             12960,3784,4609,5527,6404,7381,8230,9127,10128,10961,
1163             211770,12531,13472,14340,15210,16146,17106,18040,18870,19660,
1164             320553,21439,22349,23240,24163,25179,25990,26884,27704,28561,
1165             429470,30384,31308,32253,33169,33986,34823,35674,36563,37488,
1166             538320,39241,40203,41072,41850,42677,43572,44421,45327,46197,
1167             647137,48078,48889,49699,50509,51388,52242,53122,54009,54909,
1168             755853,56681,57485,58309,59149,59999,60871,61740,62665,63600,
1169             864482,65283,66136,66973,67847,68685,69595,70535,71427,72309,
1170             973169,73967/
1171              DATA ICAL/
1172             12950,3552,4214,4759,5470,6138,6751,7447,8097,8741,
1173             29432,10092,10759,11385,12022,12677,13309,13954,14595,15237,
1174             315869,16542,17229,17884,18539,19172,19807,20429,21043,21658,
1175             422336,23003,23691,24421,25080,25675,26300,26906,27497,28159,
1176             528805,29446,30200,30873,31525,32210,32799,33388,34069,34661,
1177             635285,36008,36647,37299,38000,38657,39345,39969,40581,41239,
1178             741886,42528,43194,43823,44472,45139,45711,46484,47156,47789,
1179             848431,49068,49688,50323,50928,51599,52247,52900,53609,54295,
1180             954920,55558,56164,56785,57421,58056,58720,59370,60023,60710,
1181             A61375,62059,62670,63269,63900,64531,65173,65822,66470,67137,
1182             B67790,68453,69120,69776,70426,71052,71690,72352,72976,73652/
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```
      FSTART=7.0
         F=(FMAX+FMIN)/1.0E+9
         IF(F.LT.4.0)FSTART=0.25
      IF(F.GT.4.0.AND.F.LT.8.0)FSTART=2.0
      IF(F.GT.8.0.AND.F.LT.14.0)FSTART=4.0
      FRE=FRE/1.0E+9
      J=(FRE-FSTART)*20.0
      FCAL=FSTART+J*0.05
      FCAL=FCAL*1.0E+9
      FRE=FRE*1.0E+9
      J=J+2
      FDIFF=0.05*1.0E+9
      IF(FMAX+FMIN.GT.4.0E+9)GO TO 5
      ICO=(FRE-FCAL)*(JCAL(J)-JCAL(J-1)+0.0)/FDIFF+JCAL(J-1)
      RETURN
    5 CONTINUE
      IF(FMAX+FMIN.GT.8.0E+9)GO TO 6
      ICO=(FRE-FCAL)*(KCAL(J)-KCAL(J-1)+0.0)/FDIFF+KCAL(J-1)
      RETURN
    6 CONTINUE
      IF(FMAX+FMIN.GT.14.0E+9)GO TO 7
      ICO=(FRE-FCAL)*(MCAL(J)-MCAL(J-1)+0.0)/FDIFF+MCAL(J-1)
      RETURN
    7 CONTINUE
      ICO=(FRE-FCAL)*(ICAL(J)-ICAL(J-1)+0.0)/FDIFF+ICAL(J-1)
      END


      SUBROUTINE TAPEGO
      IMPLICIT COMPLEX(S)
      COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
     1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
     2,CL2,ICA2,MPRT,PAD(18)
      COMMON ICOM(20)
      COMMON S(50,26)
      COMMON/PROGSET/LCOUNT,MAGMKR,NEND,NOCAL,KMKR,LMKR
      COMMON/TAPE/NTITLE(2),NTAPE,NAR,NCOM,NDATE(4),NS,NF,NPOINT
      DIMENSION NT(2)
      DATA NT/'DATATAPE'/
C     REWIND TAPE
1     CONTINUE
S        LI,1     F:112
S        AW,1     =X'01000000'
S        CAL1,1   1
C     READ AND CHECK HEADER
2     CALL BUFFER IN(112,1,NTITLE,12,I)
      IF(I-2)30,4,30
4     IF(NTITLE(1)-NT(1))40,6,40
6     IF(NTITLE(I)-NT(2))40,8,40
8     IF(NAR-2600)40,10,40
10    IF(NCOM-90)12,12,40
12    IF(NCOM-70)40,14,14
14    CALL SKIPFILE(112,2)
      CALL SKIPFILE(112,-1)
      CALL SKIPREC(112,-2)
      CALL BUFFER IN(112,1,NFILE,1,I)
      IF(I-2)30,16,30
16    CALL BUFFER IN(112,1,S,1,I)
      IF(I-2)30,18,30
18    NS=NFILE
      NF=NFILE
      NPOINT=NF+1
      MAGMKR=2
```

```
25*       S        LI,9      IDATE
26*       S        AW,9      =8Z10000000
27*       S        CAL1,8    9
28*            CALL WT(19,'DATA TAPE LOADED : ',NTAPE)
29*            CALL WTNL(16,'  NO. RECORDS = ',NF)
30*       20   RETURN
31*       C    READ ERR
32*       30   CALL WT(43,'READ ERROR ON TAPE. REPLACE TAPE OR ABANDON')
33*            CALL CHOOSE(16,' (TYPE R OR A) !',1,'REPLACE,ABANDON;',I)
34*            CALL WTNL
35*            GO TO(45,20)I
36*            GO TO 30
37*       C    WRONG TAPE
38*       40   CALL WTNL(44,'WRONG TAPE LOADED. DO YOU WISH TO CORRECT ? ')
39*            CALL CHOOSE(15,'(TYPE Y OR N) !',1,'YES,NO;',J)
40*            CALL WTNL
41*            GO TO(45,20)J
42*            GO TO 40
43*       45   IBC=-1
44*            CALL RDNL(37,'TYPE ANY CHARACTER WHEN TAPE RELOADED',IBC,A)
45*            GO TO 1
1244           END

1245           SUBROUTINE DUMPER
1246           IMPLICIT COMPLEX(S)
1247           COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOK,NOZ,
  1*          1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CAC,CB2
  2*          2,CL2,ICA2,MPRT,PAD(18)
1250           COMMON ICOM(20)
125.           COMMON S(50,26)
  1*           COMMON/PROGSET/LCOUNT,MAGMKR,NEND,NOCAL,KMKR,LMKR
1252           COMMON/TAPE/ATITLE(2),NTAPE,NAR,NCOM,NDATE(4),NS,NF,NPOINT
  1*           IF(MAGMKR-2)30,1,30
  2*      1    NFILE=NF+1
1253           IF(NFILE-NPOINT)20,10,2
  1*      2    CALL SKIPFILE(112,1)
  2*           CALL SKIPFILE(112,-1)
  3*           NPOINT=NF+1
1258      10   CALL BUFFER OUT(112,1,NFILE,NCOM,I)
  1*           IF(I-2)40,12,40
  2*      12   CALL BUFFER OUT(112,1,S,NAR,I)
  3*           IF(I-2)40,14,40
  4*      14   END FILE 112
  5*           END FILE 112
  6*           CALL SKIPFILE(112,-2)
1260           CALL WTNL(28,'READINGS DUMPED AS FILE NO. ',NFILE)
1261           NPOINT=NPOINT+1
1263           NF=NF+1
1264           RETURN
  1*      20   CALL WTNL(27,'TAPE COUNT LOST - RELOADING')
  2*           CALL TAPEGO
  3*           GO TO 1
  4*      30   CALL WTNL(19,'NO DATA TAPE LOADED')
  5*           RETURN
  6*      40   CALL WTNL(35,'WRITE ERROR ON TAPE. TAPE UNLOADING')
  7*           CALL SKIPFILE(112,-1)
  8*           CALL SKIPFILE(112,0)
  9*           MAGMKR=1
1288           END

1289           SUBROUTINE UNDUMP
```

```
1270              IMPLICIT COMPLEX(S)
1271              COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
   1*            1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
   2*            2,CL2,ICA2,MPRT,PAD(18)
1274              COMMON ICOM(20)
1275              COMMON S(50,26)
   1*             COMMON/PROGSET/LCOUNT,MAGMKR,NEND,NOCAL,KMKR,LMKR
1276              COMMON/TAPE/NTITLE(2),NTAPE,NAR,NCOM,NDATE(4),NS,NF,NPOINT
   1*             IF(MAGMKR-2)40,1,40
   2*       1     IBC=8
1278              CALL RDNL(40,'RECORD NO. REQUIRED (ZERO GIVES NEXT) = ',IHC,N)
1279              IF(N)12,2,4
1280       2      N=NPOINT
1281       4      IF(N-NF)10,10,20
1282       6      IF(NPOINT-LT.(2*N))GO TO 7
1283              CALL SKIPFILE(112,0)
1284              NPOINT=1
1285              GO TO 10
1286       7      BACKSPACE 112
1287              BACKSPACE 112
1288              NPOINT=NPOINT-1
1289              IF(N-NPOINT)7,12,8
   1*       8     CALL SKIPREC(112,2)
1292              NPOINT=NPOINT+1
1293       10     IF(N-NPOINT)6,12,8
1294       12     CALL BUFFER IN(112,1,NFILE,NCOM,I)
   1*             IF(I-2)30,14,30
   2*       14    CALL BUFFER IN(112,1,S,NAR,I)
   3*             IF(I-2)30,16,30
   4*       16    NPOINT=NPOINT+1
   5*             CALL WTNL(80,IARRAY)
1298              RETURN
   1*       20    CALL WTNL(20,'RECORD NO. TOO LARGE')
   2*             RETURN
   3*       30    CALL WTNL(34,'READ ERROR ON TAPE. TAPE UNLOADING')
   4*             CALL SKIPFILE(112,-1)
   5*             CALL SKIPFILE(112,0)
   6*             MAGMKR=1
   7*             RETURN
   8*       40    CALL WTNL(19,'NO DATA TAPE LOADED')
1300              END

1301              SUBROUTINE TAPEEND
1302              IMPLICIT COMPLEX(S)
1303              COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
   1*            1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
   2*            2,CL2,ICA2,MPRT,PAD(18)
1306              COMMON ICOM(20)
1307              COMMON S(50,26)
   1*             COMMON/PROGSET/LCOUNT,MAGMKR,NEND,NOCAL,KMKR,LMKR
1308              COMMON/TAPE/NTITLE(2),NTAPE,NAR,NCOM,NDATE(4),NS,NF,NPOINT
   1*             IF(MAGMKR-2)30,1,30
   2*       1     CALL SKIPFILE(112,-1)
   3*             CALL SKIPFILE(112,0)
1310              IF(NF-NS)20,15,5
1311       5      DO 7 I=1,4
1312       7      NDATE(I)=IDATE(I)
1313              N=NF-NS
1314              NS=NF
1315              CALL BUFFER OUT(112,1,NTITLE,50,I)
1316              CALL WTNL(22,'NO. OF FILES DUMPED = ',N)
1317              CALL SKIPFILE(112,0)
```

```
     1*        15    CALL WTNL(17,'DATA TAPE REWOUND')
     2*              MAGMKR=1
  1319               RETURN
  1320        20    CALL WTNL(15,'TAPE COUNT LOST')
     1*              RETURN
     2*        30    CALL WTNL(19,'NO DATA TAPE LOADED')
  1321               END

  1322               SUBROUTINE REWSPOOL
  1323               REWIND 110
  1324               RETURN
  1325               END

  1326               SUBROUTINE DESPOOL
  1327               IMPLICIT COMPLEX (S)
  1328               COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
  1329              1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
  1330              2,CL2,ICA2,MPRT,PAD(18)
  1331               COMMON ICOM(20)
  1332               COMMON S(50,26)
  1333               CALL BUFFER IN(110,1,NFILE,90,I)
  1334        5      DO 6 L=23,26
  1335        6      CALL BUFFER IN(110,1,S(1,L),100,I)
  1336               END

  1337               SUBROUTINE PRSPOOL
  1338               IMPLICIT COMPLEX (S)
  1339               COMMON NFILE,IDATE(4),IARRAY(20),FMIN,FMAX,FINC,SCENT,NOF,LOW,NOZ,
  1340              1KJOY,LL,II,IN,K,NAMP,IBOX,IT,CB1,ITYP,ICA1,ZERO,CA1,CL1,CA2,CB2
  1341              2,CL2,ICA2,MPRT,PAD(18)
  1342               COMMON ICOM(20)
  1343               COMMON S(50,26)
     1*              COMMON/PROGSET/LCOUNT,MAGMKR,NEND,NOCAL,KMKR,LMKR
  1345               IF(LCOUNT.EQ.23)GO TO 20
  1346               LCOUNT=LCOUNT+1
  1347               CALL BUFFER OUT(110,1,NFILE,90,I)
  1348               DO 5 L=23,26
  1349        5      CALL BUFFER OUT(110,1,S(1,L),100,I)
  1350               DO 10 L=1,20
  1351        10     ICOM(L)=8240404040
  1352               IF(LCOUNT.EQ.23)GO TO 15
  1353               RETURN
  1354        15     CALL WTNL(44,'WARNING - DISC FILE FULL. CLEAR WITH TASK DC')
  1355               RETURN
  1356        20     CALL WTNL(33,'DISC OVERFLOW - DATA NOT RECORDED')
  1357               END

  1358               SUBROUTINE BACKWAIT
     1*              COMMON/PROGSET/LCOUNT,MAGMKR,NEND,NOCAL,KMKR,LMKR
     2*              LOGICAL BGDPROG
  1360               CALL WTNL(16,'WAITING TO PRINT')
  1361       123     CALL ONESEC
  1362               DO 122 L=1,30
  1363               CALL WAIT
     1*              IF(BGDPROG(1))GO TO 122
  1367               GO TO 125
  1368       122     CONTINUE
  1369               CALL STOPSEC
  1370       124     CALL WTNL(46,'BACKGROUND JOB RUNNING. DO YOU WISH TO WAIT ? ')
```

```
1371            CALL CHOOSE(15,'(TYPE Y OR N) ',1,'YES,NO',L)
1372            CALL WTNL
1373            GO TO(123,126)L
1374            GO TO 124
1375      126   LCOUNT=0
1376            RETURN
1377      125   CALL STOPSEC
1378            CALL WTNL(19,'PRINTING COMMENCING')
1379            END
```

APPENDIX 2. Listing of data file tapes

Shown in this listing are details of data files dumped onto magnetic tape following measurements made using the 2-port programme listed in Appendix 1. Using the same programme any of the data files may be recalled and the results examined or recalculated in different ways.

Each measurement run record is identified by number, date, frequency range, number of measurement points and contains details of calibration configuration and values together with the measurement title.

The listings shown represent over 600 measurement runs, mostly for GaAs FET devices, at frequencies in the range 0.4 to 12GHz. This information which has been instrumental in the development of small signal GaAs FETs may be of interest to others considering the design of microwave circuits around such devices.

DATA TAPE 1 AT 10:40 JUL 25,'76

NCOM = 70 NAR = 2600 NS = 354

REC NO.	DATE WRITTEN	MIN FREQ	MAX FREQ	NO. PTS	PORT1 CAL	OFF1	OFF2 /CAP	PORT2 CAL	OFF1	OFF2 /CAP	THROUGH LENGTH	IDENTIFICATION
1	13:16 JAN 30	4.00	8.00	21	1	.350	.150	1	.350	.150	.0000	THROUGH SHIM LINE IN LID MOUNT.
2	13:16 JAN 30	4.00	8.00	21	1	.350	.150	1	.350	.150	.0000	OPEN CIRCUIT LID MOUNT.
3	13:16 JAN 30	4.00	8.00	21	1	.350	.150	1	.350	.150	.0000	OPEN CIRCUIT LID IN MOUNT.
4	13:16 JAN 30	4.00	8.00	21	1	.350	.150	1	.350	.150	.0000	LID WITH PORT 1 WIRE BONDED SHORT & PORT 2 OPEN CIRCUIT IN MOUNT.
5	13:16 JAN 30	4.00	8.00	21	1	.350	.150	1	.350	.150	.0000	388H/EB/LID/1 5V 0V I(DS)=34 MA.
6	13:30 FEB 05	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	THROUGH LINE
7	13:30 FEB 05	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	CAL. SHORT
8	13:30 FEB 05	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	O/C H-P TRANSISTOR MOUNT
9	13:30 FEB 05	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	2780/STRIPLINE/TEST 5V 0V I(DS)=68 MA.
10	13:30 FEB 05	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	0.35 CM STRIPLINE OFFSET SHORT (PORT 2)
11	13:30 FEB 05	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	SHIM SHORT PORT 1
12	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	LID PORT 1 S/C PORT2 O/C.
13	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	380C/LID/10 5V 0V I(DS)=13 MA.
14	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	380C/LID/11 5V 0V I(DS)=33.5 MA.
15	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	380C/LID/12 5V 0V I(DS)=23 MA.
16	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	380C/LID/13 5V 0V I(DS)=31.5 MA.
17	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/1 5V 0V I(DS)=35 MA.
18	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/2 5V 0V I(DS)=45 MA.
19	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/2 3V 0V I(DS)=48 MA.
20	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/2 7V 0V I(DS)=43 MA.
21	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/2 5V 0V I(DS)=43 MA.
22	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/3 5V 0V I(DS)=57 MA.
23	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/3 5V 0V I(DS)=42.5 MA.
24	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/3 7V 0V I(DS)=5[illegible] MA.
25	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/3 5V -1V I(DS)=50 MA.
26	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/3 5V -2V I(DS)=42.5 MA.
27	12:34 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	3268/LID/7 5V 0V I(DS)=28.5 MA.
28	16:53 FEB 07	.40	2.00	17	1	.000	.150	1	.000	.150	.0000	THROUGH LINE IN LID MOUNT.
29	16:53 FEB 07	.40	2.00	17	1	.000	.150	1	.000	.150	.0000	LID WITH PORT 1 S/C AND PORT 2 O/C.
30	16:53 FEB 07	.40	2.00	17	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/1 5V 0V I(DS)=35 MA.
31	16:53 FEB 07	.40	2.00	17	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/2 5V 0V I(DS)=45.5 MA.
32	16:53 FEB 07	.40	2.00	17	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/2 5V 0V I(DS)=43 MA.
33	16:53 FEB 07	.40	2.00	17	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/3 5V 0V I(DS)=58 MA.
34	17:23 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	LID WITH PORT 1 S/C AND PORT 2 O/C.
35	17:23 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/1 5V 0V I(DS)=35 MA.
36	17:23 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/2 5V 0V I(DS)=45.5 MA.
37	17:23 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/2 5V 0V I(DS)=43 MA.
38	17:23 FEB 07	2.00	4.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/3 5V 0V I(DS)=58 MA.
39	17:48 FEB 07	4.00	8.00	21	1	.000	.150	1	.000	.150	.0000	LID WITH PORT 1 S/C AND PORT 2 O/C.
40	17:48 FEB 07	4.00	8.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/1 5V 0V I(DS)=35 MA.
41	17:48 FEB 07	4.00	8.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/2 5V 0V I(DS)=45.5 MA.
42	17:48 FEB 07	4.00	8.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/2 5V 0V I(DS)=43 MA.
43	17:48 FEB 07	4.00	8.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/3 5V 0V I(DS)=57.5 MA.
44	18:12 FEB 07	8.00	12.00	21	1	.000	.150	1	.000	.150	.0000	THROUGH LINE IN LID MOUNT.
45	18:12 FEB 07	8.00	12.00	21	1	.000	.150	1	.000	.150	.0000	LID WITH PORT 1 S/C AND PORT 2 O/C.
46	18:12 FEB 07	8.00	12.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/1 5V 0V I(DS)=35 MA.
47	18:12 FEB 07	8.00	12.00	21	1	.000	.150	1	.000	.150	.0000	3888/EB/LID/2 5V 0V I(DS)=45.5 MA.
48	18:12 FEB 07	8.00	12.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/2 5V 0V I(DS)=43 MA.
49	18:12 FEB 07	8.00	12.00	21	1	.000	.150	1	.000	.150	.0000	390C/EB/LID/3 5V 0V I(DS)=57.5 MA.
50	12:40 FEB 21	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	THROUGH CONNECTION COAXIAL SYSTEM.
51	12:40 FEB 21	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	PORT 1 OPEN CIRCUIT. PORT 2 SHORT CIRCUIT.
52	12:40 FEB 21	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	MICROSTRIP TEST PIECE PORT 1 TO "A" PORT 2 TO "

												B".
53	12:40	FEB 21	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	10 CM. AIR LINE.
54	19:16	FEB 27	2.00	4.00	21	1	-.250	.040	1	-.250	.040	.0000	THROUGH SHIM OFFSET=-0.25CM. CAPACITANCE =0.0. PF.
55	19:16	FEB 27	2.00	4.00	21	1	-.250	.040	1	-.250	.040	.0000	LID WITH PORT 1 S/C PORT 2 O/C.
56	19:16	FEB 27	2.00	4.00	21	1	-.200	.040	1	-.200	.040	.0000	380C/LID/19 5V 0V I(DS)=19.5 MA. (OFFSET =-0. 2 CAPACITANCE =0.04 PF).
57	19:16	FEB 27	2.00	4.00	21	1	-.200	.040	1	-.200	.040	.0000	380C/LID/22 5v 0V I(DS)=20.5 MA.
58	19:16	FEB 27	2.00	4.00	21	1	-.200	.040	1	-.200	.040	.0000	380C/LID/23 5v 0V I(DS)=19 MA.
59	19:16	FEB 27	2.00	4.00	21	1	-.200	.040	1	-.200	.040	.0000	380C/LID/24 5v 0V I(DS)=21 MA.
60	19:16	FEB 27	2.00	4.00	21	1	-.200	.040	1	-.200	.040	.0000	380C/LID/25 5v 0V I(DS)=8.5 MA.
61	19:16	FEB 27	2.00	4.00	21	1	-.200	.040	1	-.200	.040	.0000	380C/LID/26 5v 0V I(DS)=21 MA.
62	19:16	FEB 27	2.00	4.00	21	1	-.200	.040	1	-.200	.040	.0000	380C/LID/27 5V 0V I(DS)=18 MA.
63	19:16	FEB 27	2.00	4.00	21	1	-.200	.040	1	-.200	.040	.0000	380C/LID/27 5V I(DS)=15 MA.
64	19:16	FEB 27	2.00	4.00	21	1	-.200	.040	1	-.200	.040	.0000	380C/LID/20 5v I(DS)=15 MA.
65	20:21	FEB 27	.40	2.00	17	1	-.200	.040	1	-.200	.040	.0000	LID WITH PORT 1 S/C PORT 2 O/C.
66	20:21	FEB 27	.40	2.00	17	1	-.200	.040	1	-.200	.040	.0000	380C/LID/19 5V 0V I(DS)=19.5 MA. (OFFSET =0. 2 CM. CAPACITANCE =0.04 PF)
67	20:21	FEB 27	.40	2.00	17	1	-.200	.040	1	-.200	.040	.0000	380C/LID/20 5v 0V I(DS)=18.5 MA.
68	20:21	FEB 27	.40	2.00	17	1	-.200	.040	1	-.200	.040	.0000	380C/LID/21 5v 0V I(DS)=21 MA.
69	20:21	FEB 27	.40	2.00	17	1	-.200	.040	1	-.200	.040	.0000	380C/LID/22 5v 0V I(DS)=20.5 MA
70	20:21	FEB 27	.40	2.00	17	1	-.200	.040	1	-.200	.040	.0000	380C/LID/23 5V 0V I(DS)=18.5 MA.
71	20:21	FEB 27	.40	2.00	17	1	-.200	.040	1	-.200	.040	.0000	380C/LID/24 5v 0V I(DS)=21.5 MA.
72	20:21	FEB 27	.40	2.00	17	1	-.200	.040	1	-.200	.040	.0000	380C/LID/25 5v 0V I(DS)=8 MA.
73	20:21	FEB 27	.40	2.00	17	1	-.200	.040	1	-.200	.040	.0000	380C/LID/27 5V 0V I(DS)=16 MA.
74	13:25	MAR 05	8.00	12.00	21	2	.000	.300	2	.000	.300	.0000	CO-AXIAL THROUGH LINE.
75	13:25	MAR 05	8.00	12.00	21	2	.000	.300	2	.000	.300	.0000	PORT 1 OPEN CIRCUIT PORT 2 APC-7 SHORT CIRCUIT .
76	13:25	MAR 05	8.00	12.00	21	2	.000	.300	2	.000	.300	.0000	MICROSTRIP TEST PIECE, PORT 1 TO "A", PORT 2 TO "B".
77	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	THROUGH SHIM IN LID MOUNT.
78	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	LID WITH PORT 1 S/C AND PORT 2 O/C.
79	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/5 5V 0V I(DS)=40 MA.
80	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/6 5V 0V I(DS)=47 MA.
81	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/7 5V 0V I(DS)=42 MA.
82	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/8 5V 0V I(DS)=34.5 MA.
83	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/9 5V 0V I(DS)=13 MA.
84	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/10 5V 0V I(DS)=12 MA.
85	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/11 5V 0V I(DS)=29.5 MA.
86	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/11 5V -1.0V I(DS)=10.5 MA.
87	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/12 5V 0V I(DS)=44 MA.
88	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/13 5V 0V I(DS)=16 MA.
89	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/14 5V 0V I(DS)=30 MA.
90	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/15 5V 0V I(DS)=43 MA.
91	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/16 5V 0V I(DS)=26.5 MA.
92	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/17 5V 0V I(DS)=61 MA.
93	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/18 5V 0V I(DS)=22 MA.
94	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/19 5V 0V I(DS)=14.5 MA.
95	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/20 5V 0V I(DS)=18 MA.
96	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/21 5V 0V I(DS)=26 MA.
97	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/22 5V 0V I(DS)=43 MA.
98	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/23 5V 0V I(DS)=16 MA.
99	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/24 5V 0V I(DS)=20MA.
100	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/25 5V 0V I(DS)=27 MA.
101	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/26 5V 0V I(DS)=23 MA.
102	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/28 5V 0V I(DS)=36 MA.
103	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/29 5V 0V I(DS)=56 MA.
104	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/30 5V 0V I(DS)=3. MA.
105	19:11	MAR 13	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/31 5V 0V I(DS)=1C MA.
106	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	THROUGH LINE (OFFSET=-0.23 CM. CAPACITANCE =0.0 3 PF).
107	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/32 5V 0V I(DS)=56 MA.
108	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/33 5V 0V I(DS)=23 MA.

109	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/34 5V 0V I(DS)=20 MA.
110	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/35 5V 0V I(DS)=51 MA.
111	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/36 5V 0V I(DS)=32 MA.
112	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/37 5V 0V I(DS)=28 MA.
113	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/38 5V 0V I(DS)=39.5 MA.
114	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/39 5V 0V I(DS)=55.5 MA.
115	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	314A/EB/LID/2 5V 0V I(DS)=34.5 MA.
116	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	314A/EB/LID/3 5V 0V I(DS)=15 MA.
117	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/1 5V 0V I(DS)=36 MA.
118	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/2 5V 0V I(DS)=47 MA.
119	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/3 5V 0V I(DS)=42.5 MA.
120	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/4 5V 0V I(DS)=49.5 MA.
121	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/5 5V 0V I(DS)=38.5 MA.
122	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/6 5V 0V I(DS)=17 MA.
123	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/7 5V 0V I(DS)=44 MA.
124	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/8 5V 0V I(DS)=45 MA.
125	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/9 5V 0V I(DS)=58 MA.
126	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/10 5V 0V I(DS)=53 MA.
127	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	388C/EB/LID/1 5V 0V I(DS)=8.2 MA.
128	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	388B/EB/LID/1 5V 0V I(DS)=38 MA.
129	12:56	MAR 26	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/9 5V 0V I(DS)=50.5 MA (AFTER "BURN-IN" PROBING).
130	12:56	MAR 26	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/EB/LID/10 5V 0V I(DS)=27 MA. (AFTER "BURN-IN" PROBING).
131	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/32 5V -4V I(DS)=20 MA.
132	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/33 5V -0.1V I(DS)=20 MA.
133	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/34 5V 0V I(DS)=18 MA.
134	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/35 5V -3.5V I(DS)=20 MA.
135	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/36 5V -0.8V I(DS)=20 MA.
136	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/37 5V -0.7V I(DS)=20 MA.
137	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/38 5V -1.8V I(DS)=20 MA.
138	19:18	MAR 20	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	390C/EB/LID/39 5V -4.2V I(DS)=20 MA.
139	14:06	APR 04	1.00	2.00	21	1	.000	.000	1	.000	.000	.0000	G-R OPEN PORT 1 G-R SHORT PORT 2.
140	14:06	APR 04	1.00	2.00	21	1	.000	.000	1	.000	.000	.0000	CRANFIELD RED P/N PORT 1 G-R OPEN PORT 2.
141	14:06	APR 04	1.00	2.00	21	1	.000	.000	1	.000	.000	.0000	CRANFIELD GREEN PORT 1 RED PORT 2.
142	14:39	APR 04	2.00	4.00	41	1	.000	.000	1	.000	.000	.0000	G-R OPEN PORT 1 G-R SHORT PORT 2.
143	14:39	APR 04	2.00	4.00	41	1	.000	.000	1	.000	.000	.0000	CRANFIELD RED P/N PORT 1 GREEN P/N PORT 2.
144	14:39	APR 04	2.00	4.00	41	1	.000	.000	1	.000	.000	.0000	CRANFIELD GREEN P/N PORT 1 RED P/N PORT 2.
145	16:13	APR 08	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	XI 1/6/LID/1 V(CE)=3V I(CE)=5 MA.
146	16:13	APR 08	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	XI 1/6/LID/1 V(CB)=0V I(CE)=5 MA.
147	16:13	APR 08	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	XI 1/6/LID/1 V(CE)=3V I(CE)=5 MA. 20DB.
148	16:13	APR 08	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	XI 1/6/LID/1 V(CB)=0V I(CE)=5 MA. 20 DB.
149	16:13	APR 08	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	XI 1/6/LID/2 V(CE)=3V I(CE)=5 MA. 20 DB.
150	16:13	APR 08	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	XI 1/1/LID/1 V(CE)=3V I(CE)=5 MA. 20 DB.
151	17:40	APR 08	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	XI 1/6/LID/1 V(CE)=3V I(CE)=5 MA. 20 DB.
152	17:40	APR 08	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	XI 1/6/LID/1 V(CB)=0V I(CE)=5 MA. 20 DB.
153	17:40	APR 08	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	XI 1/6/LID/2 V(CE)=3V I(CE)=5 MA. 20 DB.
154	17:40	APR 08	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	XI 1/1/LID/1 V(CE)=3V I(CE)=5 MA. 20 DB.
155	17:40	APR 08	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	XI 1/1/LID/1 V(CE)=3V I(CE)=0.5 MA. 20 DB.
156	13:28	APR 09	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	OPEN PORT 1 SHORT PORT 2
157	13:28	APR 09	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	SHORT PORT 1 .3 OFFSET PORT 2
158	13:28	APR 09	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	.46 OFFSET PORT 1 1.16 OFFSET PORT 2
159	13:28	APR 09	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	FIXED LOAD PORT 1 SLIDING LOAD PORT 2
160	13:28	APR 09	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	MATCH LOADS REVERSED
161	12:53	APR 19	4.00	8.00	41	2	.000	.465	2	.000	.465	.0000	THROUGH CONNECTION (CO-AXIAL SYSTEM).
162	12:53	APR 19	4.00	8.00	41	2	.000	.465	2	.000	.465	.0000	PORT 1 APC-7 OPEN CIRCUIT PORT 2 APC-7 SHORT CIRCUIT.
163	12:53	APR 19	4.00	8.00	41	2	.000	.465	2	.000	.465	.0000	MICROSTRIP TEST PIECE "A" TO PORT 1 "B" TO PORT 2.
164	12:53	APR 19	4.00	8.00	41	2	.000	.465	2	.000	.465	.0000	MICROSTRIP TEST PIECE REVERSED "B" TO PORT 1.
165	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	THRU LINE
166	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	372C/LID/20 5V 0V I(DS)=22 MA. GAT 2 DEVICE.
167	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	372C/LID/20 5V 0V I(DS)=22 MA. REPEAT THRU LI

													E REMOVED.
68	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	372C/LID/21 5V 0V I(DS)=21.5MA.
69	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	372C/LID/22 5V 0V I(DS)=25 MA.
70	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	372C/LID/23 5V 0V I(DS)=21 MA.
71	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	372C/LID/24 5V 0V I(DS)=28.5 MA.
72	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/7 5V 0V I(DS)=58 MA. GAT 2 DEVICE.
73	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/8 5V 0V I(DS)=67 MA.
74	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/8 5V 0V I(DS)=67 MA.
75	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/9 5V 0V I(DS)=60 MA.
76	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/10 5V 0V I(DS)=45 MA.
77	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/11 5V 0V I(DS)=48 MA.
78	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/12 5V 0V I(DS)=62.5 MA.
79	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/13 5V 0V I(DS)=66 MA.
80	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/14 5V 0V I(DS)=75 MA.
81	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/15 5V 0. I(DS)=55 MA.
82	10:48	APR 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	3560/LID/16 5V 0V I(DS)=60 MA.
83	12:44	APR 30	4.00	8.00	41	2	.000	.465	2	.000	.465	.0000	CO-AX THRU LINE.
84	12:44	APR 30	4.00	8.00	41	2	.000	.465	2	.000	.465	.0000	MICROSTRIP TEST PIECE. "A" TO PORT 1 , "B" TO PORT 2.
85	12:44	APR 30	4.00	8.00	41	2	.000	.465	2	.000	.465	.0000	MICROSTRIP TEST PIECE (REVERSED). "B" TO PORT 1 .
86	12:44	APR 30	4.00	8.00	41	2	.000	.465	2	.000	.465	.0000	PORT 1 APC-7 OPEN CIRCUIT, PORT 2 SHORT CIRCUIT .
87	12:16	APR 30	7.10	12.00	50	2	.000	.300	2	.000	.300	.0000	CO-AX THRU LINE.
88	12:16	APR 30	7.10	12.00	50	2	.000	.300	2	.000	.300	.0000	MICROSTRIP TEST PIECE. "A" TO PORT 1, "B" TO PO RT 2.
89	12:16	APR 30	7.10	12.00	50	2	.000	.300	2	.000	.300	.0000	MICROSTRIP TEST PIECE (REVERSED). "B" TO PORT 1 .
90	12:16	APR 30	7.10	12.00	50	2	.000	.300	2	.000	.300	.0000	PORT 1 APC-7 OPEN CIRCUIT, PORT 2 SHORT CIRCUI .
91	12:36	JUL 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/1 5V 0V I(DS)=39 MA.
92	12:36	JUL 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/4 5V 0V I(DS)=48 MA.
93	12:36	JUL 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	419A/LID/3 5V 0V I(DS)=16 MA.
94	12:36	JUL 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	419A/LID/4 5V 0V I(DS)=17.5 MA.
95	12:36	JUL 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/7 5V 0V I(DS)=41 MA.
96	12:36	JUL 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/8 5V 0V I(DS)=18 MA.
97	12:36	JUL 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/9 5V 0V I(DS)=21.5 MA.
98	12:36	JUL 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/10 5V 0V I(DS)=17 MA.
99	12:36	JUL 25	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	388C/EB/LID/1 5V 0V I(DS)=7.5 MA.
00	13:22	JUL 30	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/11 5V 0V I(DS)=37 MA.
01	13:22	JUL 30	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/12 5V 0V I(DS)=35 MA.
02	13:22	JUL 30	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/13 5V 0V I(DS)=33 MA.
03	13:22	JUL 30	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	417A/LID/14 5V 0V I(DS)=30 MA.
04	13:22	JUL 30	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	388C/LID/(AFTER COUPLING IN S-BAND AMP. J=J+/1) 5 V 0V I(DS)=16 MA.
05	13:22	JUL 30	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	422A/LID/3 5V 0V I(DS)=32 MA.
06	13:22	JUL 30	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	422A/LID/2 5V 0V I(DS)=20 MA.
07	13:22	JUL 30	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	100 PF CHIP CAPACITOR (MILRAMAR) IN LID JIG.
08	12:32	AUG 06	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/1 5V 0V I(DS)=31 MA.
09	12:32	AUG 06	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/2 5V 0V I(DS)=29 MA.
10	12:32	AUG 06	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/3 5V 0V I(DS)=26 MA.
11	12:32	AUG 06	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/5 5V 0V I(DS)=35 MA.
12	12:32	AUG 06	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/7 5V 0V I(DS)=38 MA.
13	12:32	AUG 06	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/8 5V 0V I(DS)=23.5 MA.
14	12:32	AUG 06	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/9 5V 0V I(DS)=25 MA.
15	12:29	AUG 06	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/1 5V 0V I(DS)=31 MA. (PHASE=GAIN INDICATOR).
16	12:29	AUG 06	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/1 5V -1.5V 15 MA. (PHASE=GAIN IND ICATOR.)
17	12:38	OCT 22	2.00	4.00	21	1	.530	.000	1	.530	.000	.0000	THROUGH LINE ON ONE INCH ALUMINA SUBSTRATE.
18	12:38	OCT 22	2.00	4.00	21	1	.530	.000	1	.530	.000	.0000	OPEN CIRCUIT ON ONE INCH ALUMINA SUBSTRATE.
19	12:38	OCT 22	2.00	4.00	21	1	.530	.000	1	.530	.000	.0000	417A/C00/1 5V 0V I(DS)=15 MA.
20	12:38	OCT 22	2.00	4.00	21	1	.530	.000	1	.530	.000	.0000	417A/C00/2 5V 0V I(DS)=26 MA.

221	12:38	OCT 22	2.00	4.00	21	1	.530	.000	1	.530	.000	.0000	OFFSET SHORT ON HALF ALUMINA SUBSTRATE.
222	12:53	OCT 29	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	CAL. THROUGH LINE.
223	12:53	OCT 29	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	10 CM. AIR LINE AND APC-7 S/C ON PORT 1. PORT 2 S/C.
224	12:53	OCT 29	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	1.16 CM. SHORT CIRCUIT ON PORT 1. SHORT CIRCUIT ON PORT 2.
225	12:53	OCT 29	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	SHORT CIRCUIT PORT 1. 1.16 CM. OFFSET SHORT PORT 2. (AS ABOVE BUT REVERSED).
226	12:53	OCT 29	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	20 CM. AIR LINE + APC-7 SHORT PORT 1. APC-7 SHORT PORT 2.
227	13:31	OCT 29	2.00	4.00	21	2	.000	.300	2	.000	.300	.0000	20 CM. AIR LINE + APC-7 SHORT PORT 1. APC-7 SHORT PORT 2.
228	13:31	OCT 29	2.00	4.00	21	2	.000	.300	2	.000	.300	.0000	20 CM. THROUGH AIR LINE.
229	13:31	OCT 29	2.00	4.00	21	2	.000	.300	2	.000	.300	.0000	ALUMINA SHORT PORT 1. ALUMINA OPEN CIRCUIT PORT 2.
230	13:31	OCT 29	2.00	4.00	21	2	.000	.300	2	.000	.300	.0000	417A/C00/2 5V 0V I(DS)=25 MA. FULL CORR. TO APC-7 CONNECTORS.
231	12:47	NOV 05	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	10 CM AIR LINE & SHORT ON PORT 1. SHORT (APC-7) PORT 2.
232	12:47	NOV 05	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	20 CM AIR LINE & S/C ON PORT 1.
233	12:47	NOV 05	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	20 CM. +10 CM.AIR LINES & 1.16 CM OFFSET SHORT ON PORT 1. APC-7 S/C PORT 2.
234	12:47	NOV 05	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	417A/C00/2 5V 0V VIDS)=26 MA. FULL CORR. TO APC-7 CONNECTORS.
235	13:17	NOV 05	4.00	8.00	21	2	.000	.300	2	.000	.300	.0000	CAL. THROUGH LINE.
236	13:17	NOV 05	4.00	8.00	21	2	.000	.300	2	.000	.300	.0000	20 CM AIR LINE & S/C ON PORT 1. APC-7 SHORT ON PORT 2.
237	13:17	NOV 05	4.00	8.00	21	2	.000	.300	2	.000	.300	.0000	20 CM AIR LINE & S/C ON PORT 1. APC-7 SHORT PORT 2. (RE-CALIBRATED.)
238	13:17	NOV 05	4.00	8.00	21	2	.000	.300	2	.000	.300	.0000	SHORT PORT 1 .46 OFFSET PORT 2
239	13:17	NOV 05	4.00	8.00	21	2	.000	.300	2	.000	.300	.0000	417A/C00/2 5V 0V I(DS)=25 MA. FULL CORR. TO APC-7 CONNECTORS.
240	13:17	NOV 05	4.00	8.00	21	2	.000	.300	2	.000	.300	.0000	10CM AIR LINE &S/C PORT 1. 1.16 CM OFFSET SHORT PORT 2.
241	13:17	NOV 05	4.00	8.00	21	2	.000	.300	2	.000	.300	.0000	S/C BOTH PORTS
242	13:34	DEC 17	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	20 CM AIR LINE PLUS S/C PORT 1. 1.16 CM OFFSET S/C PORT 2. PGI.
243	13:34	DEC 17	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	1.16 CM OFFSET S/C PORT 1. 20 CM AIR LINE PLUS S/C PORT 2. PGI.
244	13:34	DEC 17	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	10 CM AIR LINE PLUS S/C PORT 1. S/C PORT 2. PG 1.
245	13:34	DEC 17	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	S/C PORT 1. 10 CM AIR LINE PLUS S/C PORT 2. PG 1.
246	13:34	DEC 17	7.20	12.00	25	2	.000	.300	2	.000	.300	.0000	CAL. THROU LINE. PGI.
247	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	CRC THROUGH LINE MOUNT.
248	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	CAL. SHORT IN CRC DEVICE MOUNT.
249	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	OPEN CIRCUIT CRC DEVICE MOUNT.
250	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	EMPTY CRC PACKAGE IN DEVICE MOUNT.
251	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	437/R/EB/CRC/7 5V 0V I(DS)=20 MA. FULL CORR. PROG.
252	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	437R/EB/CRC/7 5V -1V I(DS)=10 MA.
253	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	437R/EB/CRC/13 5V 0V I(DS)=11.5 MA.
254	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	429R/EB/CRC/13 5V 0V I(DS)=16 MA.
255	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	429R/EB/CRC/13 5V -0.5V I(DS)=10 MA.
256	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	429R/EB/CRC/14 5V 0V I(DS)=18 MA.
257	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	429R/EB/CRC/14 5V -0.75V I(DS)=10 MA.
258	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	429R/EB/CRC/16 5V 0V I(DS)=15.5 MA.
259	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	429R/EB/CRC/16 5V -0.6V I(DS)=10 MA.
260	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	437R/EB/CRC/10 5V 0V I(DS)=18.5 MA.
261	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	437R/EB/CRC/10 5V -1.0V I(DS)=10 MA.
262	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	437R/EB/CRC/11 5V 0V I(DS)=10.5 MA.
263	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	437R/EB/CRC/8 5V 0V I(DS)=19 MA.
264	12:41	DEC 31	2.00	4.00	21	1	.010	.035	1	.010	.035	.0000	437R/EB/CRC/8 5V -1.0V I(DS)=10 MA.

265	12:41	DEC 31	2:00	4:00	21	1	.010	.035	1	.010	.035	.0000	437H/EB/CRC/9 5V 0V I(DS)=11 MA.
266	20:21	FEB 27	:40	2:00	17	1	-.230	.030	1	-.230	.030	.0000	380C/LID/27 5v 0V I(DS)=16 MA.
267	11:34	JAN 09	2:00	4:00	21	1	.330	.030	1	.330	.030	.0000	CAL. THROUGH LINE.
268	11:34	JAN 09	2:00	4:00	21	1	.330	.030	1	.330	.030	.0000	417A/LID/7 5v 0V I(DS)=40 MA. POLYGUIDE TEST SUBSTRATE.
269	11:34	JAN 09	2:00	4:00	21	1	.330	.030	1	.330	.030	.0000	417A/LID/7 5v 0V I(DS)=40 MA. POLYGUIDE TEST SUBSTRATE.
270	19:16	FEB 27	2:00	4:00	21	1	-.230	.030	1	-.230	.030	.0000	380C/LID/27 5V I(DS)=15 MA.
271	16:53	FEB 07	:40	2:00	17	1	-.230	.030	1	-.230	.030	.0000	388B/EB/LID/1 5V 0V I(DS)=35 MA.
272	17:23	FEB 07	2:00	4:00	21	1	-.230	.030	1	-.230	.030	.0000	388B/EB/LID/1 5V 0V I(DS)=35 MA.
273	17:48	FEB 07	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	388H/EB/LID/1 5V 0V I(DS)=35 MA.
274	18:12	FEB 07	8:00	12:00	21	1	-.230	.030	1	-.230	.030	.0000	388B/EB/LID/1 5V 0V I(DS)=35 MA.
275	16:53	FEB 07	:40	2:00	17	1	-.230	.030	1	-.230	.030	.0300	388H/EB/LID/1 5V 0V I(DS)=35 MA.
276	17:23	FEB 07	2:00	4:00	21	1	-.230	.030	1	-.230	.030	.0300	388H/EB/LID/1 5V 0V I(DS)=35 MA.
277	17:48	FEB 07	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0300	388H/EB/LID/1 5V 0V I(DS)=35 MA.
278	18:12	FEB 07	8:00	12:00	21	1	-.230	.030	1	-.230	.030	.0300	388B/EB/LID/1 5V 0V I(DS)=35 MA.
279	12:48	JAN 21	2:00	4:00	21	1	-.330	.020	1	-.330	.020	.0000	POLYGUIDE CAL. THROUGH LINE.
280	12:48	JAN 21	2:00	4:00	21	1	-.330	.020	1	-.330	.020	.0000	417A/LID/7 5V 0V I(DS)=40 MA. POLYGUIDE 100 OHM TEST PIECE.
281	12:48	JAN 21	2:00	4:00	21	1	-.330	.020	1	-.330	.020	.0000	456A/EB/LID/3 5V 0V I(DS)=16 MA. POLYGUIDE 100 OHM TEST PIECE.
282	12:48	JAN 21	2:00	4:00	21	1	-.330	.020	1	-.330	.020	.0000	401A/EB/2 5V 0V I(DS)=29 MA. POLYGUIDE 100 OHM TEST PIECE.
283	12:48	JAN 21	2:00	4:00	21	1	-.330	.020	1	-.330	.020	.0000	OPEN CIRCUIT POLYGUIDE 100 OHM TEST PIECE.
284	12:48	JAN 21	2:00	4:00	21	1	-.330	.020	1	-.330	.020	.0000	100 OHM TEST PIECE PORT 1. CAL. OFFSET S/C PORT 2.
285	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	CAL. THROUGH LINE IN LID JIG.
286	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	EMPTY LID JIG.
287	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/3 5V 0V I(DS)=26 MA. H-P LID MOUNT.
288	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/6 5V 0V I(DS)=26.5 MA.
289	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/7 5V 0V I(DS)=16.5 MA.
290	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/8 5V 0V I(DS)=12 MA.
291	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/9 5V 0V I(DS)=20 MA.
292	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/10 5V 0V I(DS)=13 MA.
293	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/11 5V 0V I(DS)=24 MA.
294	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/12 5V 0V I(DS)=15.5 MA.
295	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/13 5V 0V I(DS)=32 MA.
296	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/14 5V 0V I(DS)=27 MA.
297	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/15 5V 0V I(DS)=21 MA.
298	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/16 5V 0V I(DS)=17 MA.
299	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/17 5V 0V I(DS)=24 MA.
300	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/18 5V 0V I(DS)=16 MA.
301	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/19 5V 0V I(DS)=6.5 MA.
302	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/20 5V 0V I(DS)=21 MA.
303	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/21 5V 0V I(DS)=22 MA.
304	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/22 5V 0V I(DS)=13 MA.
305	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/23 5V 0V I(DS)=11.5 MA.
306	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/24 5V 0V I(DS)=26 MA.
307	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/25 5V 0V I(DS)=22.5 MA.
308	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/26 5V 0V I(DS)=13 MA.
309	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/27 5V 0V I(DS)=39 MA.
310	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/28 5V 0V I(DS)=20 MA.
311	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/29 5V 0V I(DS)=18.5 MA.
312	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/30 5V 0V I(DS)=18 MA.
313	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/31 5V 0V I(DS)=18 MA.
314	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/32 5V 0V I(DS)=15 MA.
315	12:36	JAN 23	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	CAL. THRU LINE.
316	12:32	JAN 29	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	CAL. THROUGH LINE.
317	12:32	JAN 29	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/3 5V 0V I(DS)=16 MA.
318	12:32	JAN 29	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/3 5V -0.7V I(DS)=10 MA.
319	12:32	JAN 29	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/4 5V 0V I(DS)=18 MA.
320	12:32	JAN 29	4:00	8:00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/4 5V -1V I(DS)=9 MA.

321	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/7 5V -0.8V I(DS)=9 MA.
322	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/8 5V -0.5V I(DS)=7 MA.
323	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/9 5V -1.0V I(DS)=10 MA.
324	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/10 5V -0.6V I(DS)=8 MA.
325	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/11 5V -1.4V I(DS)=11 MA.
326	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/12 5V -0.6V I(DS)=10 MA.
327	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/14 5V -1.7V I(DS)=10 MA.
328	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/15 5V -1.2V I(DS)=10 MA.
329	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/16 5V -1.0V I(DS)=7 MA.
330	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/17 5V -1.5V I(DS)=10 MA.
331	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/ER/LID/20 5V -1.2V I(DS)=8 MA.
332	12:32	JAN 29	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/21 5V -1.2V I(DS)=8 MA.
333	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	CAL. THROUGH LINE IN LID MOUNT.
334	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/22 5V -0.3V I(DS)=10 MA.
335	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/26 5V -0.5V I(DS)=7 MA.
336	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/27 5V -2.6V I(DS)=16 MA.
337	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/28 5V -0.7V I(DS)=13 MA.
338	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/29 5V -1.0V I(DS)=8 MA.
339	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/30 5V -0.8V I(DS)=10 MA.
340	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	456A/EB/LID/31 5V -1.0V I(DS)=8 MA.
341	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/19 5V -0.5V I(DS)=10 MA.
342	12:32	JAN 30	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	401A/EB/LID/21 5V 0V I(DS)=14.5 MA.
343	12:08	JUL 24	12.50	16.50	21	2	.000	.300	2	.000	.300	.0000	CAL. THROUGH LINE.
344	12:08	JUL 24	12.50	16.50	21	2	.000	.300	2	.000	.300	.0000	S/C PORT1. .465 CM OFFSET SHORT PORT 2.
345	12:08	JUL 24	12.50	16.50	21	2	.000	.300	2	.000	.300	.0000	MATCHED LOAD PORT 1. .3 CM CAL. OFFSET SHORT PORT 2.
346	12:08	JUL 24	12.50	16.50	21	2	.000	.300	2	.000	.300	.0000	1.16 CM OFFSET SHORT PORT 1. 10 CM AIR LINE PLUS S/C PORT 2.
347	12:58	JAN 14	2.00	4.00	21	1	-.330	.020	1	-.330	.020	.0000	417A/LID/7 5V 0V I(DS)=40 MA. POLYGUIDE 100 OHM TEST PIECE.
348	12:58	JAN 14	2.00	4.00	21	1	-.330	.020	1	-.330	.020	.0000	CAL. THROUGH LINE (REPEAT).
349	12:58	JAN 14	2.00	4.00	21	1	-.330	.020	1	-.330	.020	.0000	417A/LID/8 5V 0V I(DS)=16.5 MA.
350	12:58	JAN 14	2.00	4.00	21	1	-.330	.020	1	-.330	.020	.0000	417A/LID/9 5V 0V I(DS)=19.5 MA.
351	12:38	JAN 16	4.00	8.00	21	1	-.330	.020	1	-.330	.020	.0000	POLYGUIDE CAL. THROUGH LINE.
352	12:38	JAN 16	4.00	8.00	21	1	-.330	.020	1	-.330	.020	.0000	456A/EB/LID/4 5V 0V I(DS)=17.5 MA. POLYGUIDE 100 OHM TEST SUBSTRATE.
353	12:38	JAN 16	4.00	8.00	21	1	-.330	.020	1	-.330	.020	.0000	456A/EB/LID/3 5V 0V I(DS)=16.5 MA. POLYGUIDE 100 OHM TEST SUBSTRATE.
354	12:38	JAN 16	4.00	8.00	21	1	-.330	.020	1	-.330	.020	.0000	401A/EB/LID/2 5V 0V I(DS)=29 MA. POLYGUIDE 100 OHM TEST SUBSTRATE.

END OF DATA

DATA TAPE 8 AT 10:45 JUL 25,'76

#COM = 90 NAK = 2600 NS = 261

REC NO.	DATE WRITTEN	MIN FREQ	MAX FREQ	NO. PTS	PORT1 CAL	OFF1	OFF2 /CAP	PORT2 CAL	OFF1	OFF2 /CAP	THROUGH LENGTH	IDENTIFICATION
1	13:18 MAY 27	2.00	4.00	21	1	.300	.020	1	.300	.020	.0000	POLYGUIDE CAL. THROUGH LINE.
2	13:18 MAY 27	2.00	4.00	21	1	.300	.020	1	.300	.020	.0000	OPEN CIRCUIT CRC POLYGUIDE TEST MOUNT.
3	13:18 MAY 27	2.00	4.00	21	1	.300	.020	1	.300	.020	.0000	437R/CRC/9 5V 0V I(DS)=13 MA.
4	13:51 MAY 27	4.00	8.00	21	1	.300	.020	1	.300	.020	.0000	POLYGUIDE CAL. THROUGH LINE.
5	13:51 MAY 27	4.00	8.00	21	1	.300	.020	1	.300	.020	.0000	OPEN CIRCUIT POLYGUIDE CRC TEST MOUNT.
6	13:51 MAY 27	4.00	8.00	21	1	.300	.020	1	.300	.020	.0000	437R/CRC/9 5V 0V I(DS)=13 MA.
7	01:50 MAY 29	2.00	4.00	21	1	.250	.000	1	.250	.000	.0000	POLYGUIDE CAL. THROUGH LINE. CB-AXIAL OFFSET CALIBRATION (0.25CM.)
8	01:50 MAY 29	2.00	4.00	21	1	.250	.000	1	.250	.000	.0000	OPEN CIRCUIT POLYGUIDE CRC TEST MOUNT.
9	01:50 MAY 29	2.00	4.00	21	1	.250	.000	1	.250	.000	.0000	OPEN CIRCUIT POLYGUIDE CRC TEST MOUNT.
10	01:50 MAY 29	2.00	4.00	21	1	.250	.000	1	.250	.000	.0000	479A/CRC/3 5V 0V I(DS)=23.5 MA.
11	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	CAL. THROUGH LINE.
12	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	S-BAND AMP. TEST POLYGUIDE SUBSTRATE (SCC) WITH 417A/CRC/2 5V 0V I(DS)=30 MA.
13	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	TEST AMP. WITH 417A/CRC/2 4V 0V I(DS)=30 MA.
14	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	TEST AMP. WITH 417A/CRC/2 3V 0V I(DS)=30.5 MA.
15	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	TEST AMP. WITH 417A/CRC/2 2V 0V I(DS)=30.5 MA.
16	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	TEST AMP. WITH 417A/CRC/2 1V 0V I(DS)=25 MA.
17	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	TEST AMP. WITH 417A/CRC/2 0V 0V I(DS)=0 MA.
18	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	S-BAND POLYGUIDE TEST AMP. WITH 417A/CRC/2 5V -0.6V I(DS)=20 MA.
19	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	TEST AMP. WITH 417A/CRC/2 5V -1.1V I(DS)=10 MA.
20	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	TEST AMP. WITH 417A/CRC/2 5V -3V I(DS)=0 MA.
21	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	CB-AX TO MICROSTRIP LAUNCHERS SHORTED TO MOUNTING BLOCK.
22	13:12 JUN 03	2.00	4.00	21	2	.000	1.160	2	.000	1.160	.0000	OPEN CIRCUIT LAUNCHERS.
23	12:24 JUL 03	4.00	8.00	21	1	1.160	.020	1	1.160	.020	.0000	CAL. POLYGUIDE THROUGH LINE.
24	12:24 JUL 03	4.00	8.00	21	1	1.160	.020	1	1.160	.020	.0000	OPEN CIRCUIT C2 POLYGUIDE TEST MOUNT.
25	12:24 JUL 03	4.00	8.00	21	1	1.160	.020	1	1.160	.020	.0000	CAL. OFFSET S/C PORT 1 CAL. O/C PORT 2.
26	13:28 JUL 11	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	THROUGH LINE.
27	13:28 JUL 11	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/17 5V 0V I(DS)=38 MA.
28	13:28 JUL 11	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/20 5V 0V I(DS)=10 MA.
29	13:28 JUL 11	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/22 5V 0V I(DS)=24 MA.
30	13:28 JUL 11	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/22 5V -1V I(DS)=10 MA.
31	13:28 JUL 11	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/22 3V 0V I(DS)=24 MA.
32	13:28 JUL 11	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/22 3V -1V I(DS)=10 MA.
33	13:28 JUL 11	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/22 3V -1.5V I(DS)=5 MA.
34	13:28 JUL 11	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	S/C 3MM LAUNCHER PORT 1. APC-7 S/C PORT 2.
35	14:10 JUL 11	2.00	4.00	21	1	-.240	.000	1	.240	.000	.0000	CAL. POLYGUIDE THROUGH LINE.
36	14:10 JUL 11	2.00	4.00	21	1	-.240	.000	1	.240	.000	.0000	479A/CRC/22 5V 0V I(DS)=24.5 MA.
37	14:10 JUL 11	2.00	4.00	21	1	-.240	.000	1	.240	.000	.0000	479A/CRC/22 5V -1V I(DS)=10 MA.
38	14:10 JUL 11	2.00	4.00	21	1	-.240	.000	1	.240	.000	.0000	OPEN CIRCUIT POLYGUIDE CRC TEST MOUNT (0.75 INCH).
39	14:10 JUL 11	2.00	4.00	21	1	-.240	.000	1	.240	.000	.0000	O/C "OLD" POLYGUIDE CRC TEST MOUNT (1.1 INCH).
40	14:10 JUL 11	2.00	4.00	21	1	-.240	.000	1	-.240	.000	.0000	O/C "OLD" POLYGUIDE CRC TEST MOUNT (1.1 INCH).

41	14:10	JUL 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	O/C "OLD" POLYGUIDE CRC TEST MOUNT (1.1 INCH).
42	14:10	JUL 11	2.00	4.00	21	1	-.250	.020	1	-.250	.020	.0000	O/C "OLD" POLYGUIDE CRC TEST MOUNT (1.1 INCH).
43	14:10	JUL 11	2.00	4.00	21	1	-.240	.000	1	-.240	.000	.0000	479A/CRC/22 5V 0V I(DS)=24.5 MA.
44	14:10	JUL 11	2.00	4.00	21	1	-.240	.000	1	-.240	.000	.0000	479A/CRC/22 5V -1V I(DS)=10 MA.
45	14:10	JUL 11	2.00	4.00	21	1	-.240	.000	1	-.240	.000	.0000	OPEN CIRCUIT POLYGUIDE CRC TEST MOUNT (0.75 INCH).
46	12:56	JUL 15	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	CAL. THROUGH CO-AX LINE.
47	12:56	JUL 15	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/22 5V 0V I(DS)=2 4 MA.
48	12:56	JUL 15	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/22 3V 0V I(DS)=2 4 MA.
49	12:56	JUL 15	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/22 3V -1V I(DS)= 10 MA.
50	12:56	JUL 15	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	TEST AMP. SCC/4 WITH 479A/CRC/22 5V -1V I(DS)= 10 MA.
51	12:56	JUL 15	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	S/C 3MM LAUNCHER PORT1. APC-7 S/C PORT2.
52	12:56	JUL 15	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	O/C POLYGUIDE 0.75 INCH CRC MOUNT PORT 1. 3MM O FFSET S/C PORT 2.
53	12:56	JUL 15	2.00	4.00	21	2	.000	.465	2	.000	.465	.0000	0.75 POLYGUIDE CRC MOUNT WITH 479A/CRC/22 5V 0V I(DS)=24.5 MA.
54	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	CAL. THROUGH LINE IN LID MOUNT.
55	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	O/C LID MOUNT.
56	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/1 5V 0V I(DS)=43 MA.
57	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/1 5V -4.7V I(DS)=1 MA.
58	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/1 5V -6V I(DS)=0.1 MA.
59	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/2 5V 0V I(DS)=29 MA.
60	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/2 5V -3V I(DS)=1 MA.
61	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/2 5V -3.5V I(DS)=0.1 MA.
62	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/3 5V 0V I(DS)=35 MA.
63	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/3 5V -3.8V I(DS)=1 MA.
64	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/3 5V -4.7V I(DS)=0.1 MA.
65	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/4 5V 0V I(DS)=49 MA.
66	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/4 5V -5V I(DS)=1 MA.
67	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/4 5V -5.5V I(DS)=0.1 MA.
68	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/5 5V 0V I(DS)=12.5 MA.
69	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/5 5V -1.7V I(DS)=1 MA.
70	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/5 5V -2.5V I(DS)=0.1 MA.
71	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/6 5V 0V I(DS)=41.5 MA.
72	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/6 5V -4.5V I(DS)=1 MA.
73	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	498A/LID/6 5V -5.1V I(DS)=0.1 MA.
74	13:51	JUL 22	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	OPEN CIRCUIT LID PACKAGE IN HOP MOUNT.
75	14:24	JUL 24	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	CAL. .65 INCH POLYGUIDE THROUGH LINE.
76	14:24	JUL 24	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	OPEN CIRCUIT .75 INCH POLYGUIDE CRC TEST MOUNT.
77	14:24	JUL 24	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	479A/CRC/22 5V 0V I(DS)=24 MA.
78	14:24	JUL 24	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	479A/CRC/22 3V 0V I(DS)=24 MA.
79	14:24	JUL 24	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/CRC/13 5V 0V I(DS)=19 MA.
80	14:24	JUL 24	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/CRC/13 3V 0V I(DS)=19.5 MA.
81	14:59	JUL 24	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	CAL. .65 INCH POLYGUIDE THROUGH LINE.
82	14:59	JUL 24	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	OPEN CIRCUIT .75 INCH POLYGUIDE CRC TEST MOUNT.
83	14:59	JUL 24	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/CRC/13 5V 0V I(DS)=19.5 MA.
84	14:59	JUL 24	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/CRC/13 3V 0V I(DS)=19.5 MA.
85	14:59	JUL 24	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	479A/CRC/22 5V 0V I(DS)=24 MA.
86	14:59	JUL 24	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	479A/CRC/22 3V 0V I(DS)=24 MA.
87	14:59	JUL 24	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	479A/CRC/22 3V -1V I(DS)=10 MA.
88	14:59	JUL 24	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/CRC/13 3V 0V I(DS)=19.5 MA.
89	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	POLYGUIDE .65 INCH THROUGH LINE.
90	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	OPEN CIRCUIT .75 INCH CRC MOUNT (PHASE GAIN IND ICATOR).
91	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	479A/CRC/22 5V 0V I(DS)=24 MA. (PHASE-GAIN IN DICATOR.)
92	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	479A/CRC/22 3V 0V I(DS)=24 MA.
93	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	479A/CRC/22 5V -1.6V I(DS)=5 MA.
94	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	479A/CRC/22 5V -1.1V I(DS)=1[illegible] MA.

95	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	429R/CRC/EB/13 5V 0V I(DS)=19.5 MA.
96	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	429R/EB/CRC/13 3V 0V I(DS)=19.5 MA.
97	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	429R/EB/CRC/13 5V -.8V I(DS)=10 MA.
98	13:55	AUG 12	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	429R/EB/CRC/13 5V -1.2V I(DS)=5 MA.
99	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	POLYGUIDE .65 INCH CAL. THROUGH LINE.
100	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/2 5V 0V I(DS)=35 MA. (GAT & MEAS. WITH PHASE GAIN INDICATOR.)
101	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/3 5V 0V I(DS)=36 MA.
102	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/3 5V 0V I(DS)=36.5 MA.
103	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/5 5V 0V I(DS)=37 MA.
104	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/6 5V 0V I(DS)=29 MA.
105	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/9 5V 0V I(DS)=37 MA.
106	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/10 5V 0V I(DS)=34 MA.
107	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/11 5V 0V I(DS)=17.5 MA.
108	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/12 5V 0V I(DS)=38 MA.
109	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/13 5V 0V I(DS)=33 MA.
110	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	496A/P103/1 5V 0V I(DS)=32 MA.
111	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	496A/P103/2 5V 0V I(DS)=25 MA.
112	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	496A/P103/3 5V 0V I(DS)=39 MA.
113	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	496A/P103/4 5V 0V I(DS)=15 MA.
114	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/P103/13 5V 0V I(DS)=20 MA.
115	12:29	AUG 19	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/2. 5V 0V I(DS)=35 MA. RE-CHECK.
116	11:31	AUG 21	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	POLYGUIDE .65 INCH CAL. THROUGH LINE. (PHASE-GAIN INDICATOR.)
117	11:31	AUG 21	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501B/P103/1 5V 0V I(DS)=22.5 MA.
118	11:31	AUG 21	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501B/P103/2 5V 0V I(DS)=19 MA.
119	11:31	AUG 21	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501B/P103/3 5V 0V I(DS)=15 MA.
120	11:31	AUG 21	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501B/P103/4 5V 0V I(DS)=10 MA.
121	11:31	AUG 21	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/P103/13 5V 0V I(DS)=19.5 MA.
122	12:05	AUG 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	POLYGUIDE .65 INCH CAL. THROUGH LINE. (PHASE-GAIN INDICATOR.)
123	12:05	AUG 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/2 5V 0V I(DS)=34 MA.
124	12:05	AUG 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/2 5V -1.8V I(DS)=10 MA.
125	12:05	AUG 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	496A/P103/1 5V 0V I(DS)=31.5 MA.
126	12:05	AUG 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	501B/P103/1 5V 0V I(DS)=22.5 MA.
127	12:05	AUG 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	501B/P103 5V -1.7V I(DS)=10 MA.
128	12:05	AUG 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	479A/P103/22 5V 0V I(DS)=24 MA.
129	12:05	AUG 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	479A/P103/22 5V -1.1V I(DS)=10 MA.
130	12:05	AUG 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/P103/13 5V 0V I(DS)=19.5 MA.
131	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	0.65 INCH POLYGUIDE CAL. THROUGH LINE. (PHASE-GAIN INDICATOR.)
132	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/11 (D) 5V 0V I(DS)=19 MA.
133	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/12 (D) 5V 0V I(DS)=28 MA.
134	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/1A 5V 0V I(DS)=20 MA.
135	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/2A 5V 0V I(DS)=23.5 MA.
136	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/3A 5V 0V I(DS)=16 MA.
137	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/4A 5V 0V I(DS)=24 MA.
138	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/5 5V 0V I(DS)=35 MA.
139	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/14 5V 0V I(DS)=63 MA.
140	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/15 5V 0V I(DS)=63 MA.
141	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/16 5V 0V I(DS)=47 MA.
142	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/17 5V 0V I(DS)=45 MA.
143	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/18 5V 0V I(DS)=51 MA.
144	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/19 5V 0V I(DS)=47.5 MA.
145	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/6 5V 0V I(DS)=20 MA.
146	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/7 5V 0V I(DS)=23 MA.
147	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/8 5V 0V I(DS)=36 MA.
148	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/9 5V 0V I(DS)=18 MA.
149	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/10 5V 0V I(DS)=20 MA.
150	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/20 5V 0V I(DS)=54 MA.
151	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/21 5V 0V I(DS)=44 MA.
152	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/22 5V 0V I(DS)=54 MA.
153	13:26	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/23 5V 0V I(DS)=34 MA.

194	15:28	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/24 5V 0V I(DS)=45 MA.
195	15:28	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/25 5V 0V I(DS)=50 MA.
196	15:28	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/9 5V 0V I(DS)=36 MA.
197	15:28	AUG 28	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/14 5V -3.1V I(DS)=25 MA.
198	12:43	OCT 02	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	.65 INCH POLYGUIDE THROUGH LINE.
199	12:43	OCT 02	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/1 5V 0V I(DS)=11 MA.
200	12:43	OCT 02	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/2 5V 0V I(DS)=24 MA.
201	12:43	OCT 02	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/3 5V 0V I(DS)=15 MA.
202	12:43	OCT 02	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/4 5V 0V I(DS)=20.5 MA.
203	12:43	OCT 02	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/5 5V 0V I(DS)=27 MA.
204	12:43	OCT 02	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/6 5V 0V I(DS)=16 MA.
205	12:43	OCT 02	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/9 5V 0V I(DS)=36 MA.
206	13:27	OCT 02	8.00	12.00	21	1	-.240	.020	1	-.240	.020	.0000	.65 INCH POLYGUIDE THROUGH LINE.
207	13:27	OCT 02	8.00	12.00	21	1	-.240	.020	1	-.240	.020	.0000	D/C P103 .75 INCH TEST SUBSTRATE.
208	13:27	OCT 02	8.00	12.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/1 5V 0V I(DS)=11 MA.
209	13:27	OCT 02	8.00	12.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/2 5V 0V I(DS)=24 MA.
210	13:27	OCT 02	8.00	12.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/3 5V 0V I(DS)=15 MA.
211	13:27	OCT 02	8.00	12.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/4 5V 0V I(DS)=20.5 MA.
212	13:27	OCT 02	8.00	12.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/5 5V 0V I(DS)=27 MA.
213	13:27	OCT 02	8.00	12.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/6 5V 0V I(DS)=15 MA.
214	12:53	OCT 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	.65 INCH POLYGUIDE THROUGH LINE.
215	12:53	OCT 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	OPEN CIRCUIT POLYGUIDE P103 MOUNT.
216	12:53	OCT 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/2 5V 0V I(DS)=24 MA.
217	12:53	OCT 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	504B/P103/3 5V 0V I(DS)=15 MA.
218	12:53	OCT 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/5 5V 0V I(DS)=35 MA.
219	12:53	OCT 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	501A/P103/6 5V 0V I(DS)=21 MA.
220	12:53	OCT 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	417A/P103/28 5V 0V I(DS)=16 MA.
221	12:53	OCT 21	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/5 5V 0V I(DS)=37 MA.
222	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	.65 INCH POLYGUIDE THROUGH LINE.
223	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	D/C POLYGUIDE P103 MOUNT.
224	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	504B/P103/2 5V 0V I(DS)=24 MA.
225	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	504B/P103/3 5V 0V I(DS)=15 MA.
226	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	501A/P103/6 5V 0V I(DS)=21.5 MA.
227	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	501A/P103/4 5V 0V I(DS)=25 MA.
228	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	417A/P103/28 5V 0V I(DS)=28 MA.
229	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	417A/P103/28 5V -0.3V I(DS)=10 MA.
230	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	500A/P103/5 5V 0V I(DS)=37 MA.
231	13:45	OCT 21	.50	2.00	16	1	-.240	.020	1	-.240	.020	.0000	500A/P103/5 5V -1.5V I(DS)=10 MA.
232	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	.65 INCH POLYGUIDE THROUGH LINE.
233	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	515A/P103/1 5V 0V I(DS)=41 MA. (N+ CONTACT DE VICE.)
234	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	515A/P103/2 5V 0V I(DS)=29 MA.
235	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	515A/P103/2 5V -1.1V I(DS)=10 MA.
236	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	508A/P103/1 5V 0V I(DS)=29 MA. (LIQUID EPI.)
237	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	509A/P103/1 5V 0V I(DS)=22 MA. (1/2 MICRON G ATE.)
238	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	509A/P103/2 5V 0V I(DS)=4.5 MA.
239	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	509A/P103/3 5V 0V I(DS)=17 MA.
240	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/5 5V 0V I(DS)=37 MA.
241	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/P103/13 5V 0V I(DS)=19 MA.
242	12:52	NOV 11	2.00	4.00	21	1	-.240	.020	1	-.240	.020	.0000	D/C .75 INCH POLYGUIDE TEST MOUNT.
243	13:50	NOV 11	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	.65 INCH POLYGUIDE THROUGH LINE.
244	13:50	NOV 11	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	515A/P103/1 5V 0V I(DS)=41 MA.
245	13:50	NOV 11	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	515A/P103/2 5V 0V I(DS)=29 MA.
246	13:50	NOV 11	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	508A/P103/1 5V 0V I(DS)=29 MA.
247	13:50	NOV 11	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	509A/P103/1 5V 0V I(DS)=22 MA.
248	13:50	NOV 11	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	509A/P103/3 5V 0V I(DS)=17 MA.
249	13:50	NOV 11	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	500A/P103/5 5V 0V I(DS)=37 MA.
250	13:50	NOV 11	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	429R/P103/13 5V 0V I(DS)=19.5 MA.
251	13:50	NOV 11	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	D/C .75 INCH POLYGUIDE TEST MOUNT.
252	12:30	DEC 05	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	THROUGH LINE IN LID MOUNT.
253	12:30	DEC 05	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	OPEN CIRCUIT LID MOUNT.
254	12:30	DEC 05	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	496A/P102/3 5V 0V I(DS)=38 MA.

215	12:30	DEC 05	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	496A.P102/4 5V 0V I(DS)=19 MA.
216	12:30	DEC 05	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	496A/P102/5 5V 0V I(DS)=33 MA.
217	12:30	DEC 05	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	496A/P102/6 5V 0V I(DS)=11 MA.
218	12:30	DEC 05	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/P102/15 5V 0V I(DS)=35 MA.
219	12:30	DEC 05	4.00	8.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/P102/17 5V 0V I(DS)=25 MA.
220	13:07	DEC 05	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	THROUGH LINE IN LID MOUNT.
221	13:07	DEC 05	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	D/C LID MOUNT.
222	13:07	DEC 05	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	496A/P102/3 5V 0V I(DS)=38 MA.
223	13:07	DEC 05	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	496A/P102/4 5V 0V I(DS)=18 MA.
224	13:07	DEC 05	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	496A/P102/5 5V 0V I(DS)=33 MA.
225	13:07	DEC 05	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	496A/P102/6 5V0 I(DS)=11 MA.
226	13:07	DEC 05	2.00	4.00	21	1	-.230	.030	1	-.230	.030	.0000	398A/P102/15 5V 0V I(DS)=35 MA.
227	13:34	DEC 05	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	THROUGH LINE IN LID MOUNT.
228	13:34	DEC 05	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	D/C LID MOUNT.
229	13:34	DEC 05	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	496A/P102/3 5V 0V I(DS)=38 MA.
230	13:34	DEC 05	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	496A/P102/4 5V 0V I(DS)=18 MA.
231	13:34	DEC 05	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	496A/P102/5 5V 0V I(DS)=33 MA.
232	13:34	DEC 05	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	496A/P102/6 5V 0V I(DS)=11 MA.
233	13:34	DEC 05	.40	2.00	17	1	-.230	.030	1	-.230	.030	.0000	398A/P102/15 5V 0V I(DS)=35 MA.
234	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	THROUGH LINE .65 INCH.
235	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	526A/P103/3 5V 0V I(DS)=31 MA.
236	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	526A/P103/3 5V -1.8V I(DS)=10 MA.
237	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	526A/P103/4 5V 0V I(DS)=20 MA.
238	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	526A/P103/4 5V -.8V I(DS)=10 MA.
239	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	527A/P103/5 5V 0V I(DS)=26 MA.
240	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	527A/P103/5 5V -1.4V I(DS)=10 MA.
241	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	527A/P103/8 5V 0V I(DS)=39 MA.
242	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	527A/P103/8 5V -3.1V I(DS)=10 MA.
243	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	527A/P103/10 5V 0V I(DS)=20 MA.
244	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	527A/P103/10 5V -0.9V I(DS)=10 MA.
245	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	526A/P103/10 5V 0V I(DS)=16 MA.
246	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	526A/P103/10 5V -0.4V I(DS)=10 MA.
247	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	526A/P103/10 5V -0.9V I(DS)=5 MA.
248	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	526A/P103/12 5V 0V I(DS)=26 MA.
249	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	531A/P103/3 5V 0V I(DS)=53 MA.
250	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	531A/P103/3 5V -2.3V I(DS)=10 MA.
251	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	531A/P103/6 5V 0V I(DS)=55 MA.
252	13:31	DEC 18	4.00	8.00	21	1	-.240	.020	1	-.240	.020	.0000	531A/P103/6 5V -2.8V I(DS)=10 MA.
253	15:59	APR 04	.40	2.00	17	1	-.240	.020	1	-.240	.020	.0000	0.65 POLYGUIDE THROUGH LINE.
254	15:59	APR 04	.40	2.00	17	1	-.240	.020	1	-.240	.020	.0000	449/P103/6 5V 0V I(DS)=40 MA.
255	15:59	APR 04	.40	2.00	17	1	-.240	.020	1	-.240	.020	.0000	449/P103/6 5V 1.-3V I(DS)=10 MA.
256	15:59	APR 04	.40	2.00	17	1	-.240	.020	1	-.240	.020	.0000	449/P103/7 5V 0V I(DS)=31 MA.
257	15:59	APR 04	.40	2.00	17	1	-.240	.020	1	-.240	.020	.0000	449/P103/7 5V -0.9V I(DS)=10 MA.
258	15:59	APR 04	.40	2.00	17	1	-.240	.020	1	-.240	.020	.0000	449/P103/8 5V 0V I(DS)=26 MA.
259	15:59	APR 04	.40	2.00	17	1	-.240	.020	1	-.240	.020	.0000	449/P103/8 5V -.6V I(DS)=10 MA.
260	15:59	APR 04	.40	2.00	17	1	-.240	.020	1	-.240	.020	.0000	536D/P103/4 5V 0V I(DS)=62 MA.
261	15:59	APR 04	.40	2.00	17	1	-.240	.020	1	-.240	.020	.0000	536D/P103/4 5V -2.2V I(DS)=10 MA.

END OF DATA

APPENDIX 3. Computer programme to determine statistical data

This short Basic language computer programme was written and run on a microcomputer system to calculate Mean and Standard Deviations of sets of s-parameter and other results.

Information is supplied in DATA statements commencing at line number 200. When run the number of samples is displayed to serve as a check on the input data. The calculated mean value of the data points and the deviations are then displayed or printed as in the RUN example shown.

```
LIST
10    REM STATS CALC PROGRAM. 29/10/78.
20    N=0: S0=0: S1=0: S2=0
30    READ X
40    IF X=0 THEN 70
50    S0=S0+X
60    N=N+1: GOTO 30
70    A=S0/N
75    PRINT "NUMBER OF SAMPLES = ",: PRINT N
80    PRINT "ARITHMETIC MEAN = ",: PRINT A
90    RESTORE
100   READ X
110   IF X=0 THEN 150
120   Y=X-A
130   S1=S1+ABS(Y): S2=S2+(Y*Y)
140   GOTO 100
150   M1=S1/N: M2=SQR(S2/N)
160   PRINT "MEAN DEVIATION = ",: PRINT M1
170   PRINT "STANDARD DEVIATION = ",: PRINT M2
180   END
200   DATA 42.7,43.4,52.8,47.6,43.9,44.7,45.7,43.7
9999  DATA 0

RUN


NUMBER OF SAMPLES =  8
ARITHMETIC MEAN =  45.5625
MEAN DEVIATION =  2.353125
STANDARD DEVIATION =  3.0902821

CUTS BASIC5

READY
```

PUBLICATIONS

The following publications have resulted from the work carried out during the course of this investigation of GaAs FETs.

I.E.E. Collcquium on 'Computer-orientated practices for Microwave Component design'. 3rd June, 1974.

ON-LINE COMPUTER CORRECTION OF GALLIUM ARSENIDE FIELD-EFFECT TRANSISTOR MEASUREMENTS

H.E.G. Luxton

The correction of any microwave measurements involves characterising a number of known terminations over the frequency range of interest and using the measured characteristics of these terminations to determine error parameters of the measurement system.

This procedure is only practical over a swept frequency range if a computer is used to make the measurements required, determine the error parameters and then use these parameters to correct the measured parameters of unknown devices. At Warwick University a XDS-Sigma 5 computer is used on-line with a Hewlett-Packard (8410A) Network Analyser to determine the s-parameters of GaAs FETs and amplifiers.

Two computer programmes have been developed to characterise devices mounted on microstrip circuits or in test jigs. The simplest makes use of two short circuit and two through line calibration runs to determine the reference plane position and system gain correction factor for each s-parameter. This routine is quick, but suffers from limited accuracy and is only suitable for use at low frequencies. For improved accuracy at frequencies up to X-band a 2-port full correction programme which requires 16 calibration runs is used.

The transistors to be characterised are mounted on alumina substrates with 50 ohm input and output lines. To calibrate the microwave system and the microstrip transistor mount a combination of microstrip and co-axial terminations are used. The transistor under test is then measured and a print out of the corrected s-parameters obtained. Various gain and stability parameters are calculated from the s-parameters, and printed out if required. This latter data is particularly useful in comparing the potential amplifier performance of different devices. Plessey Gallium Arsenide field-effect transistors with 1 micron gate lengths have been characterised over X-band using this system. The predicted gain of 6 dB at 11 GHz for these devices has been investigated by using tuning elements on the microstrip mount to realise the predicted matched parameters. Two such substrates gave gains of 5.5 dB and 4.5 dB at 11.2 GHz.

When cascaded a gain of 9.0 dB was obtained; however, the measured s-parameters of the cascaded pair indicated that the output was not properly matched and predicted a gain of 12 dB. Subsequent adjustment of the output tuning resulted in a good output match with a gain of 11.5 dB.

Good agreement between the predicted and measured gain parameters is observed; however, even with the full correction calibration some residual errors are observed in the s-parameters, particularly in the phase angles of s_{11} and s_{22}. These errors are due to the imperfections of the

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calibrating terminations and variations in the device test substrates. New ways of improving the system calibration and the test mounts are being investigated to facilitate the accurate s-parameter characterisation of stripline microwave devices.

Proceedings of the European Microwave Conference, Sept. 1974.
Montreux.

GALLIUM ARSENIDE FIELD EFFECT TRANSISTORS - THEIR PERFORMANCE AND APPLICATION UP TO X-BAND FREQUENCIES

H.E.G. LUXTON

ABSTRACT

The microwave performance of GaAs FET's is reviewed and examples of their application in systems operating up to X-band frequencies discussed. Examples of amplifiers (one giving 42 dB gain at 11.2 GHz) and oscillators operating at frequencies hitherto unattainable by 2-port solid state devices are used to illustrate the performance and potential of GaAs FET's in microwave systems.

DEVICE PERFORMANCE

Gallium arsenide field effect transistors with gate lengths of 1 μm or less are currently being produced in various laboratories throughout the World [1] - [3] . These devices exhibit cut-off frequencies in excess of 30 GHz and power gains of 10 dB at X-band frequencies. Such devices are now commercially available together with 2 μm and 4 μm gate length types suitable for operation up to C and L-band frequencies respectively.

These devices have been developed principally for small signal, low noise amplifier applications. At 10 GHz the noise figure of 1 μm gate length device is typically 6 dB. At S-band 2 μm gate length devices give 10 dB of gain with a 3 dB noise figure. Similar gains and noise figures are obtained from 4 μm devices at L-band.

MICROWAVE AMPLIFIER APPLICATIONS

At frequencies below 6 GHz the GaAs FET has to compete with bipolar microwave transistors and, although it requires more careful matching, the FET offers a number of advantages at frequencies down to L-band. These are:

1. Low noise figure and high gain
2. Low intermodulation and cross-modulation distortion
3. Large dynamic range
4. Ease of d.c. biasing, which simplifies the microwave circuit design
5. High radiation resistance and thermal stability since the device is unipolar.

The low noise and distortion of the GaAs FET has led to its use in amplifiers for S-band radar and L-band receiver systems. It is, however, at X-band frequencies that the GaAs FET is unique, being capable of yielding gains of 10 dB per device at 8 GHz with output power levels of approximately +10 dBm. The small variation of the device parameters with temperature results in slight changes in the gain of amplifiers as the

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ambient temperature varies. If this gain variation cannot be tolerated by the rest of the system it may be corrected by compensation of the d.c. bias conditions.

TABLE I

GaAs FET MICROWAVE AMPLIFIERS

Description	Number and Gatelength of devices	Gain	-1dB Bandwidth	Noise Figure
L-band lumped component	1 4 μm	15dB	700MHz - 900MHz	3dB
L-band distributed element	1 4 μm	12dB	1.3GHz - 1.6GHz	3.5dB
S-band distributed element	4 2 μm	30dB	2.7GHz - 3.1GHz	3.7dB
C-band distributed, tuned	2 1 μm	15dB	5.8GHz - 6.4GHz	7.5dB
X-band distributed, tuned	3 1 μm	20dB	11.0GHz - 11.5GHz	12dB

The performance of a range of GaAs FET amplifiers is listed in Table I. All the devices were operated with zero gate and +5 volts drain-source bias. The amplifiers were optimised for gain and frequency response and the noise figures are those of the completed amplifier including input isolator, when used.

The L- and S-band amplifiers were designed using the measured s-parameters of the FET's to determine the characteristics of the matching networks required. At X-band frequencies there are problems in accurately measuring s-parameters and also in realising specific matching networks on alumina microstrip circuits. To avoid these difficulties X-band amplifier modules have been produced by using a tuning technique. This requires virtually no circuit design and no precise s-parameter data for the devices being used.

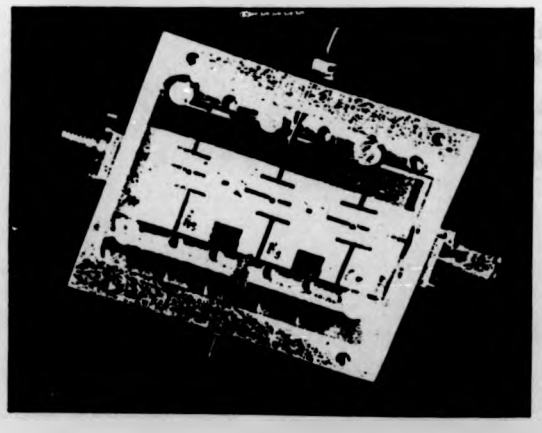


Figure 1

X-band amplifier construction

An 11.2 GHz amplifier module constructed using this technique is shown in Figure 1. Three 1 μm gate length devices mounted on discs attached to the ground plane of the alumina substrate are interconnected by lengths of 50 ohm microstrip lines. GaAs chip capacitors at the ends of these lines isolate the d.c. bias which is applied via bond wires from the microstrip bias "tees". The resistive film attached to the gate bias networks introduces loss at out of band frequencies hence stabilising the devices and preventing low frequency oscillation. Metal discs are positioned on the 50 ohm interconnecting lines to obtain the required gain response. When the optimum response has been achieved the discs are permanently fixed to the substrate.

This versatile method of construction is ideally suited to producing prototype amplifiers amplifiers and for evaluating devices. It is quick, cheap, and tolerant of device parameter variations, yet capable of realising the full potential of the FET's being used.

Figure 2

42 dB Gain

11.2 GHz GaAs FET amplifier

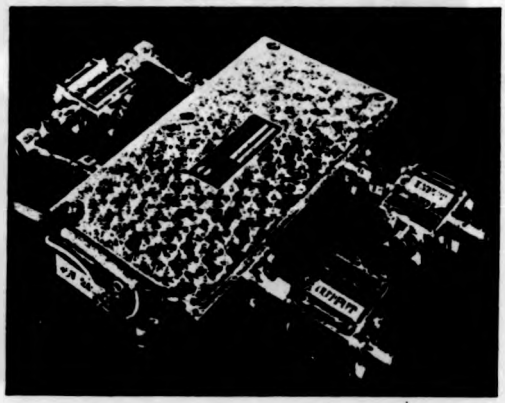
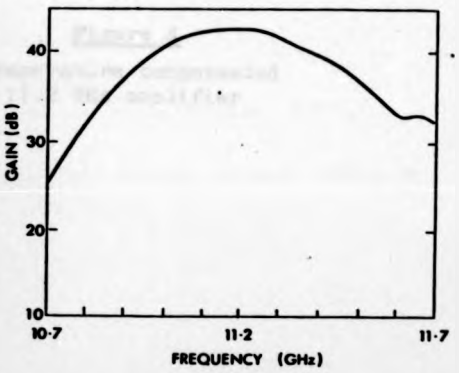


Figure 3

11.2 GHz amplifier gain response



A prototype 42 dB gain 11.2 GHz amplifier has been developed for a satellite repeater application which uses two tuned modules, Figure 2.

The gain response of this amplifier is shown in Figure 3 and other parameters are listed in Table II. This amplifier has no provision for compensating the small gain variation with temperature.

TABLE II

11.2 GHz AMPLIFIER PERFORMANCE

Centre frequency	11.18 GHz
Bandwidth at -1 dB points	260 MHz
Gain } at 20°C	42 dB
Noise figure } at 20°C	13.5 dB
Input and Output VSWR's	1.5
Gain variation 7°C - 35°C	± 1.2 dB
Third order intermodulation level at output for two equal carriers at input of -50 dBm each	- 40 dB
Output power level	8.5dBm

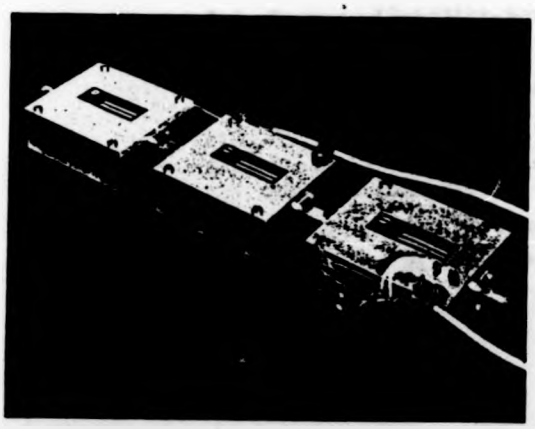


Figure 4

Temperature compensated 11.2 GHz amplifier

A three module amplifier of similar performance but incorporating a thermistor circuit to control the negative gate bias applied to the first module has also been produced, Figure 4. This reduces the gain variation with temperature to less than 1 dB total with the minimum gain occurring at 20°C.

OTHER APPLICATIONS

The GaAs FET can be used in microwave oscillator circuits. Preliminary designs at L- and X-band have given output powers of 10 mW and 5 mW with efficiencies of 20% and 10% respectively. Because the FET is a high impedance device, it does not lower the Q of the oscillator resonant circuit hence signals of good spectral purity are obtained.

At S-band the performance of 2 um gate length devices as mixers has also been examined. [4]

CONCLUSION

It has been shown that GaAs FET's may be used to produce high gain, low noise microwave amplifiers, suitable as solid state replacements for travelling wave tube and other conventional amplifiers in microwave systems.

A novel method of constructing X-band amplifier modules and compensating the gain variation with temperature has been presented.

ACKNOWLEDGEMENTS

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I.E.E. Colloquium on 'The design and application of Microwave Transistors'. 27th November, 1974.

THE PERFORMANCE AND APPLICATION OF GaAs F.E.T.s

H. E. G. Luxton

Gallium arsenide field effect transistors having cut-off frequencies in excess of 30 GHz and power gains of 10 dB at X-band frequencies are now available.

For the first time it is possible to produce small signal solid state X-band amplifiers using these FETs with advantages in performance over alternative forms of amplifier. The reliability and output power level far exceeds that of tunnel diode amplifiers. The gain variation with temperature is much less and can be easily compensated compared to solid state reflection type amplifiers. The weight and d.c. power requirements of FET amplifiers are less than travelling wave tube and other conventional microwave amplifiers.

These points are illustrated by the results obtained with amplifiers which were developed for a satellite repeater application. One consisted of two modules each containing three FETs and gave an overall gain of 42 dB at 11.2 GHz with an unoptimised noise figure of 13.5 dB. Other results for this amplifier will be presented.

The gain variation with temperature has been reduced in a three module amplifier of similar performance by incorporating a thermistor circuit to control the negative gate bias applied to the first module. This reduces the gain variation with temperature to less than 1 dB total with the minimum gain occurring at 20°C.

These X-band amplifier modules were produced using a tuning technique which avoids the problems in accurately measuring the FET s-parameters and realising specific matching networks on alumina microstrip circuits. These difficulties have since been extensively investigated and single stage X-band amplifier designs derived from the measured device s-parameters are being successfully realised.

Although it is at X-band frequencies that the GaAs FET is unique, it is being increasing used in low noise amplifiers at frequencies down to L-band. At frequencies below 6 GHz the GaAs FET has to compete with bipolar microwave transistors and, although it requires more careful matching the FET offers a number of advantages, notably low noise and low distortion performance.

The performance of a range of GaAs FET amplifiers is listed in Table 1. All the devices were operated with zero gate and +5 volts drain-source bias. The amplifiers were optimised for gain and frequency response and the noise figures are those measured for the completed amplifier including input isolator, when used.

Allen Clark Research Centre, The Plessey Company Limited, Caswell, Towcester, Northants, England.

Table 1. GaAs FET Microwave Amplifiers

Description	Number and Gatelength of devices	Gain	-1dB Bandwidth	Noise Figure
L-band lumped component	1 4 μm	15dB	700MHz - 900MHz	3dB
L-band distributed element	1 4 μm	12dB	1.3GHz - 1.6GHz	3.5dB
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C-band distributed tuned	2 1 μm	15dB	5.8GHz - 6.4GHz	7.5dB
X-band distributed	3 1 μm	20dB	11.0GHz - 11.5GHz	12dB

In addition to it's amplifier application, the performance of the GaAs FET in low power oscillator and mixer circuits is being investigated. GaAs FET oscillators operating at 3GHz giving output powers of 25 mW with efficiencies 30% have been produced and the development of a high efficiency X-band oscillator suitable for local oscillator applications is proceeding.

Presented at I.E.E. Conference on Trends in On-line Computer Control Systems (Sheffield) 21 - 24 April 1975.

APPLICATIONS OF AN ON-LINE COMPUTER IN MICROWAVE INSTRUMENTATION

H.V. Shurmer, H.E.G. Luxton and Catherine A. Stoneman

Introduction

In May 1968 R.A. Hackborn described in outline the first automatic network analyser system[1]. This cue was almost immediately taken up at Warwick University, from whom a contribution on the subject was published in May 1969[2]. In November of the following year results for two systems already tried out at Warwick were presented at a London conference[3].

Automatic network analyser measurements are now playing a major role in both national and international calibration work using packaged systems which include the computer[4]. At Warwick, meanwhile, we have continued to develop systems based on computers intended for process control which are available within the University Engineering Department, in conjunction with an assemblage of separate component items centred around the Hewlett-Packard network analyser Type 8410. This was at first a severe limitation, as the only computer then available required to be programmed in machine language and had limited peripherals. Some four years ago, however, an XDS Sigma 5 control computer became available within the Engineering Department, which offered facilities far superior to those of the packaged computers referred to above. This improved facility has been continuously employed for microwave instrumentation work over the past four years. Fig. 1 shows a photograph of the microwave network analyser system.

The main activities to date have been based on the computer correction of microwave measurements and we shall confine our paper to this subject, although the work is currently being extended into the area of computer-aided design. With computer correction, errors inherent in the system, together with those arising from transitions, mounting arrangements, etc., are first stored in the computer during a series of preliminary calibration runs, in which standard terminations are used, such as a short-circuit or a matched load[5][6][7]. During these preliminary runs, the corresponding reflection or transmission coefficients, as measured by the network analyser, are stored by the computer for a succession of precise frequency steps over a pre-selected bandwidth. Since their true impedances are accurately known, from these stored values the sum of errors at each frequency can be computed. Subsequent runs, using test pieces to be characterised, are carried out at the same precise frequency steps. The computer errors, stored at the time of the calibration runs, can be subtracted from the measured data to give a corrected output stepped over the entire predetermined bandwidth.

The Sigma 5 computer fulfils three basic requirements in the system, viz:

1. Control of the measurement procedure
2. Storage and processing of data to obtain the corrected results
3. Presentation of output data

The computer performs operations as instructed by the operator via a V.D.U.

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(Visual Display Unit) with an input keyboard. The network analyser is sited remotely from the computer and a limited number of data or control channels (10) are available for sharing between individual units, apart from the separate V.D.U. channels. This restriction has necessitated multiplexing of some of the lines.

Control of the Network Analyser

Upon receipt of the appropriate command, the computer selects the s-parameter corresponding to the desired reflection or transmission measurement. It then sets the frequency and reads the output from the network analyser. These functions require the interface units illustrated in Fig. 2, which shows a block diagram of the present system arrangement.

The s-parameter selector circuit interprets the level of an analogue voltage as a 3-bit binary word, required by the s-parameter test set. By this procedure a single analogue line serves for three digital lines.

Control of the multiplexed sweep oscillator is achieved via both the R.F. unit selector and the precision programmable voltage source. The former operates on a principle similar to that of the s-parameter selector in that a 4-bit binary word required to select one of three R.F. units is generated from a single analogue voltage. The programmable voltage source controls the output frequency of the selected R.F. unit. To facilitate this, the normal ramp tuning voltage has been removed and instead the programmable voltage source supplies a voltage which can be increased progressively in steps of 1 mV over the range 3 V to 73 V, corresponding to the full frequency range of each of the R.F. units. Each step of voltage is determined by calibration data stored in the computer. Three separate lines from the computer are required for the operation of this unit. These respectively provide initialization, output and cancellation of the tuning voltage.

Once a particular frequency is set up it is read by the automatic frequency counter. The reading may be fed back to the computer along a single channel by converting the counter output from eight parallel bits into serialized form. A second channel is used to carry both positive and negative analogue voltages, which serve either as clock pulses for the serializer or control instructions for the counter. A detailed schematic circuit of the interface units is shown in Fig. 3.

The output from the network analyser to the computer comprises two analogue voltages, corresponding to the real and imaginary parts of the parameter measured, which are transmitted via buffer amplifiers. The latter serve to improve the signal to noise ratios at the analogue inputs of the computer.

In the present system, nine of the ten available channels are employed. Work is however proceeding on the introduction of a phase-locked loop system to improve both the frequency accuracy and frequency stability of the microwave sources. This will require at least two channels and, to keep the total number within the ten available, the inputs to the programmable voltage source will be multiplexed.

Introduction of the phase-locking system can be expected to result in an extension of the measurement read times, since a finite time is required

at each frequency step for the locking to occur. At present the interval between each measurement is 0.3s and the pause at the start of each sweep over the frequency bandwidth is 2s. This is just sufficient to allow all transient effects in the system to have died away by the time each set of readings from the network analyser is transmitted to the computer. The present total time for automatic measurement of the four s-parameters of a two-port device over 50 frequency steps is 100s.

Programming

The Sigma 5 computer was recently extended to have 32 K storage capacity, which is backed by a R.A.D. (rapid access disc) of 1.5 Megabytes, each byte being a quarter of a 32-bit computer word. The core storage is divided between foreground and background areas. Tasks in the foreground area are executed according to a priority interrupt system, the background being used for batch processing.

Programming for the Sigma 5 is in Fortram IV and for present purposes the programme is written as a series of subroutines. Preparation is on punched cards, followed by transfer to magnetic tape. The user controls the programme by means of a series of questions or instructions together with answers or responses, the former being posed on the V.D.U. and the operator replying via the keyboard. A typical question would be: "Length of off-set short circuit?" and a typical instruction: "Connect short circuit at Port 1". In either case the programme is arranged so that the computer waits until a suitable reply has been received before proceeding. There are four main sections to the programme:-

1) Initialization. This part poses a series of questions to the operator, so as to allow the setting of the environment for the particular run, including calibration options and frequency ranges.

2) Calibration. The operator is requested to connect a series of standard terminations. Measurements for each termination are then made over the specified frequency ranges and the results stored by the computer.

3) Measurement, Correction and Display. On completion of the calibration procedures the operator is requested to connect the D.U.T. (device under test). This is then measured, the results corrected in accordance with the calibration data and displayed either graphically on the V.D.U. or in tabular form via the line printer. This stage may be repeated for any number of D.U.T.'s.

4) Task. This section allows flexibility in running the programme. A list of options is offered which permit parameters to be changed, calibration data to be re-read and basic sequences to be re-entered at various points. A facility is provided whereby the results may be dumped on to magnetic tape in a "photographic" manner, i.e. a complete image of the data store is copied. This can be re-loaded, remotely from the network analyser system, enabling facilities to be used which core limitations have precluded from the main programme, thus permitting more sophisticated graphical plots or tabulations of results.

A considerable degree of overlaying has now been incorporated into the

programme, so as to facilitate its use in a time-sharing environment, by reducing the core storage employed and allowing extended running time. To this end the programme itself has been written as a series of subroutines, arranged into a hierarchical structure of control and functional parts. This arrangement is also desirable in allowing greater flexibility in the content of the programme, which is demanded by the research environment in which it finds its application. One specific example is the ability to substitute one calibration routine for another, dependent on the particular circuit environment of the D.U.T.

The overlay structure enables the programme to be operated within 8 K of core store, including a section reserved as data store. The main control or root section branches into four sub-sections:-

a) Calibration and Reading Control. Calls correction and reading routines.

b) Line Printer Routine. Available for tabulated results.

c) V.D.U. Display Control. Calls graph plotting routines.

d) Initialization and Task Control. Calls data set-up, initialization, tape dumping routines, etc.

Application to the Measurement of Microwave F.E.T.'s

The major application of the facility so far has been in the development of microwave field-effect transistors for use in microstrip transmission lines. Accurate measurements would be impossible without such a system of correction because of the difficulties of characterising the transitions to the transistor mounts. The labour and time involved in attempting such measurements without computer aid would be prohibitive.

In addition to the general advantages, the system offers some especially attractive features in relation to the characterisation of F.E.T.'s. For instance, the effects of cross-coupling between ports of the test fixtures may be eradicated. This is particularly advantageous in measuring the reverse transmission, which is very small but important in relation to stability. The definition of reference-plane positions is facilitated, a provision of extreme value when using asymmetric mounts or a coaxial "flexible arm". Rapid comparison of D.U.T.'s is facilitated by the addition of subroutines to calculate gain and stability, which presents little problem with the present programme structure.

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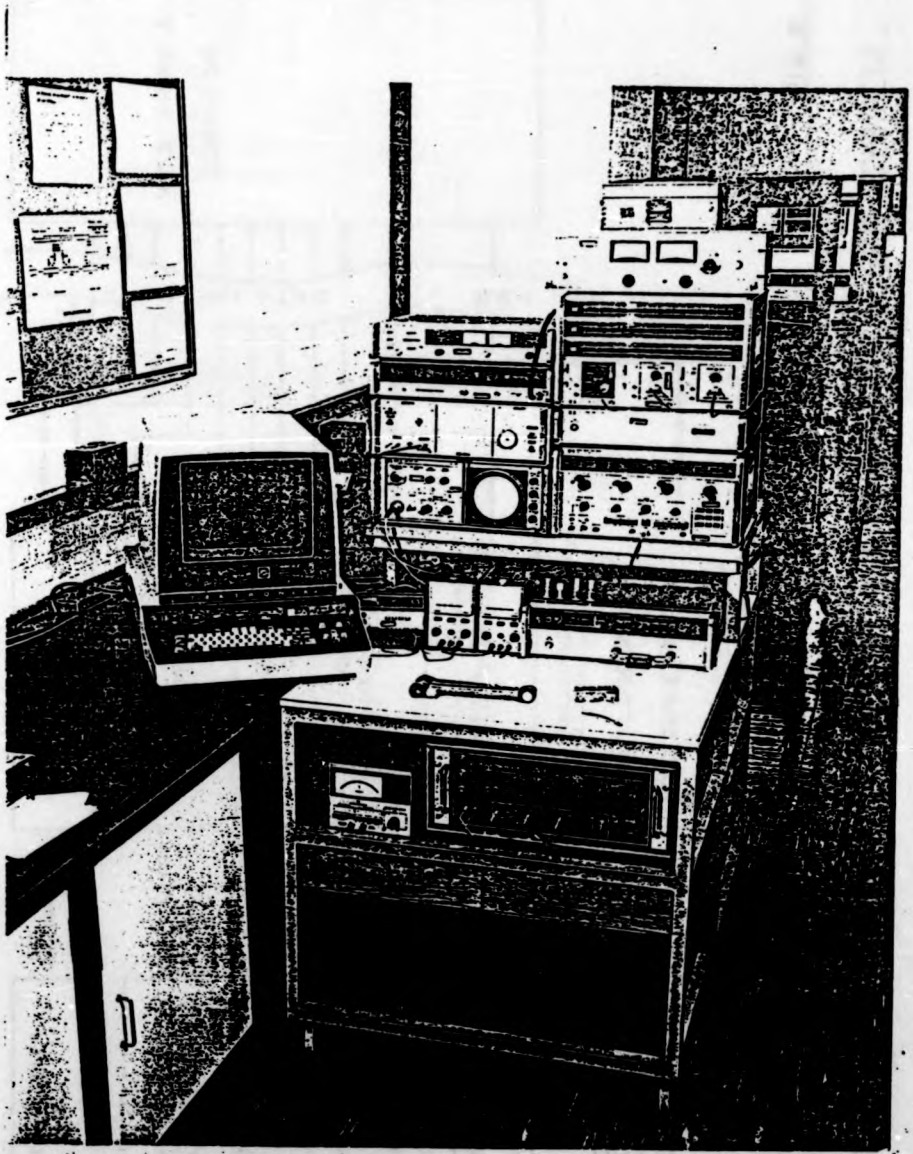


FIG. 1.

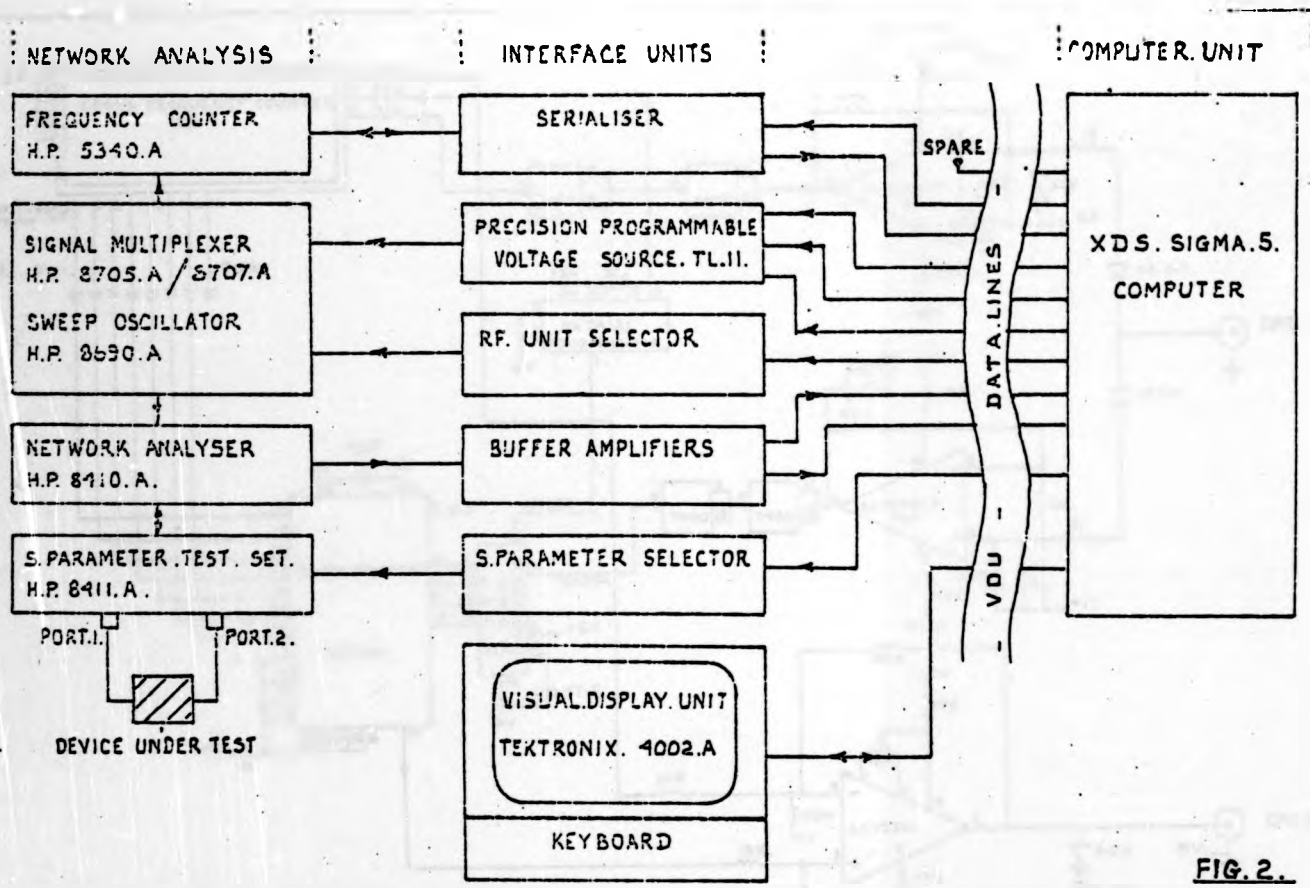
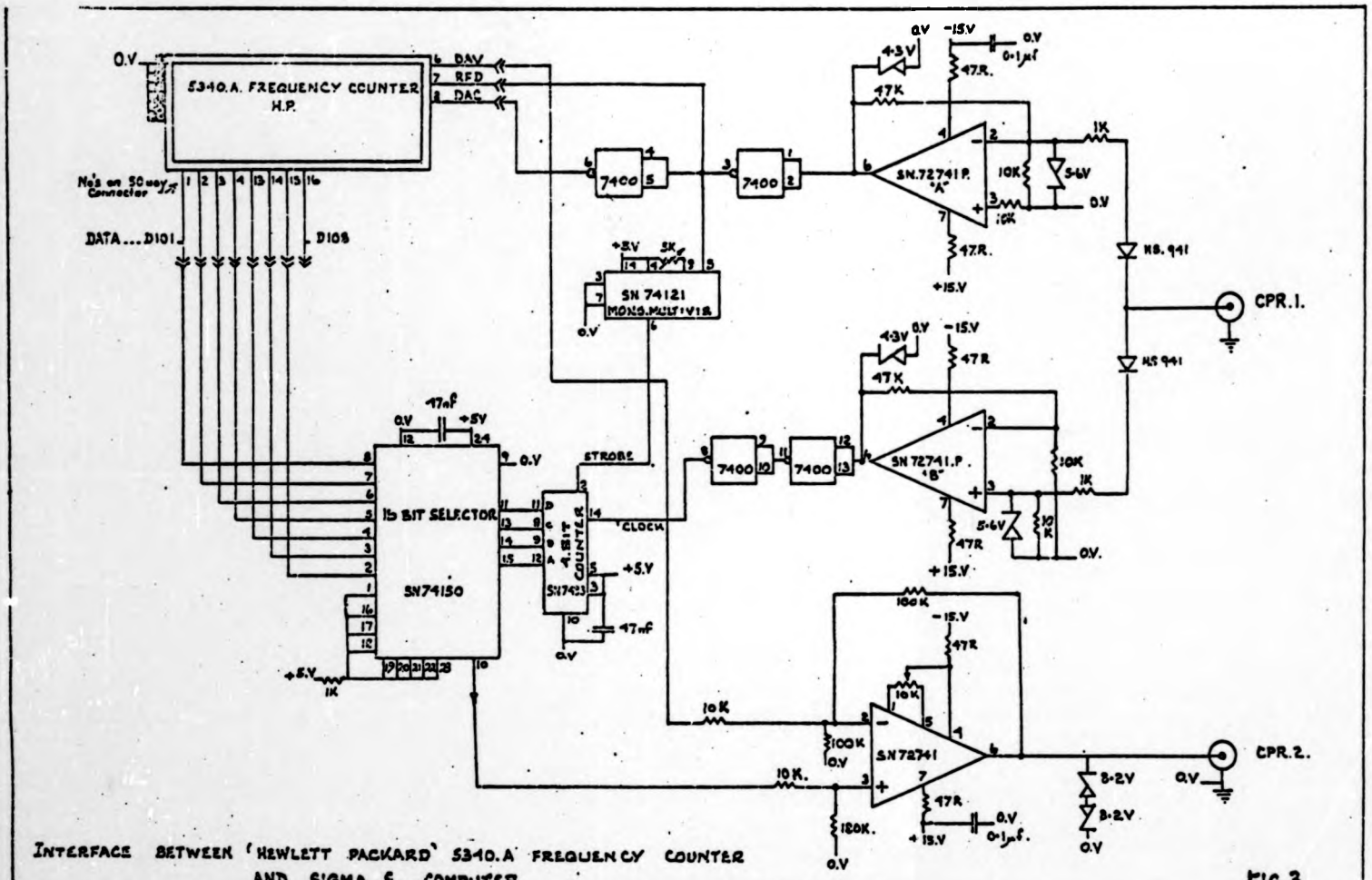


FIG. 2.

BLOCK DIAGRAM OF COMPUTER CORRECTED MICROWAVE ANALYSER SYSTEM..



INTERFACE BETWEEN 'HEWLETT PACKARD' 5340.A FREQUENCY COUNTER AND SIGMA.5. COMPUTER

FIG.3.